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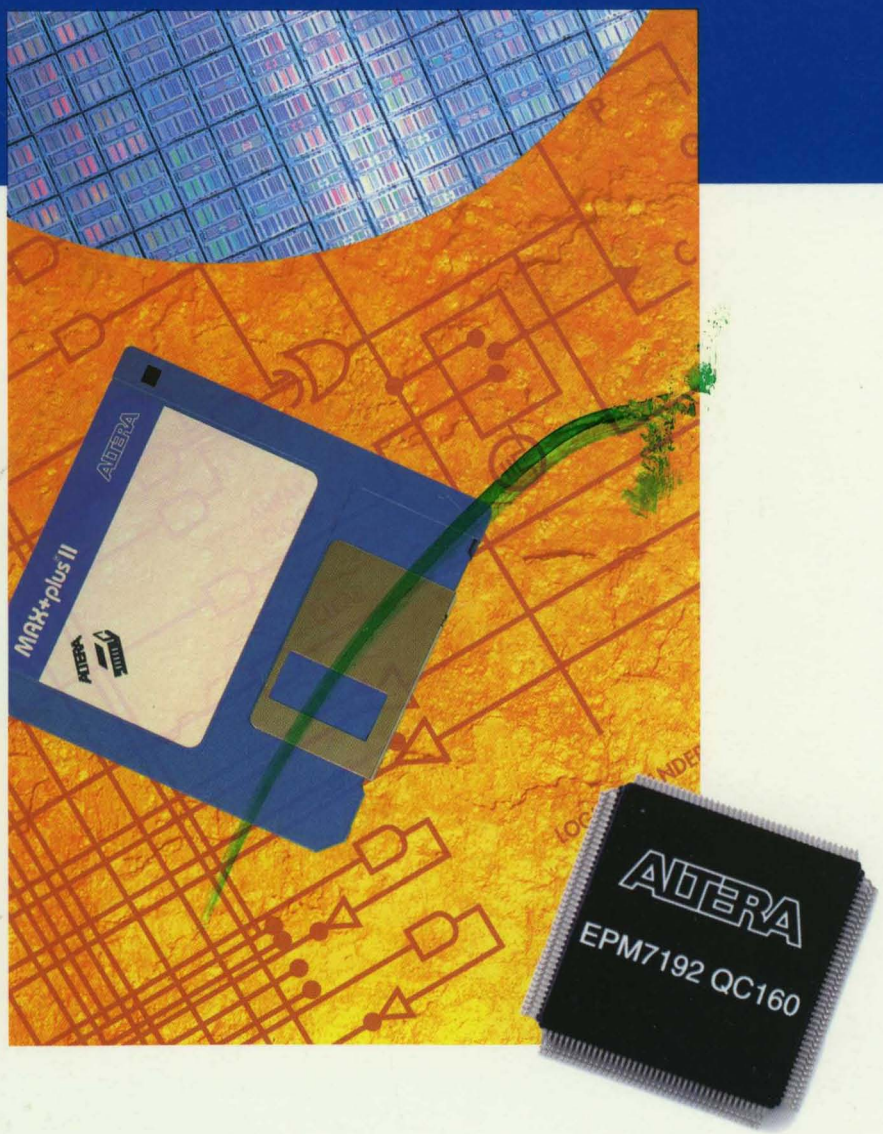

MAX 7000 Data Book

MAX 7000
Data Book

February 1993

MAX 7000 Data Book
February 1993 A-DB-M700093-0

About this Data Book

February 1993

This data book provides comprehensive information about Altera's MAX 7000 devices and MAX+PLUS II development tools. For information on Classic, MAX 5000/EPS464, and EPS448 devices, see the Altera 1992 ***Data Book***. For information on FLEX 8000 devices, see the *FLEX 8000 Programmable Logic Device Family Data Sheet*. For information on Micro Channel EPLDs and the MCMap development system, refer to the Altera ***Micro Channel Adapter Handbook***.

For immediate assistance on technical questions, call the Altera Applications Hotline:

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For information on product availability, pricing, and order status, contact your local Altera representative or distributor listed in *Sales Offices, Distributors & Representatives* in this data book.

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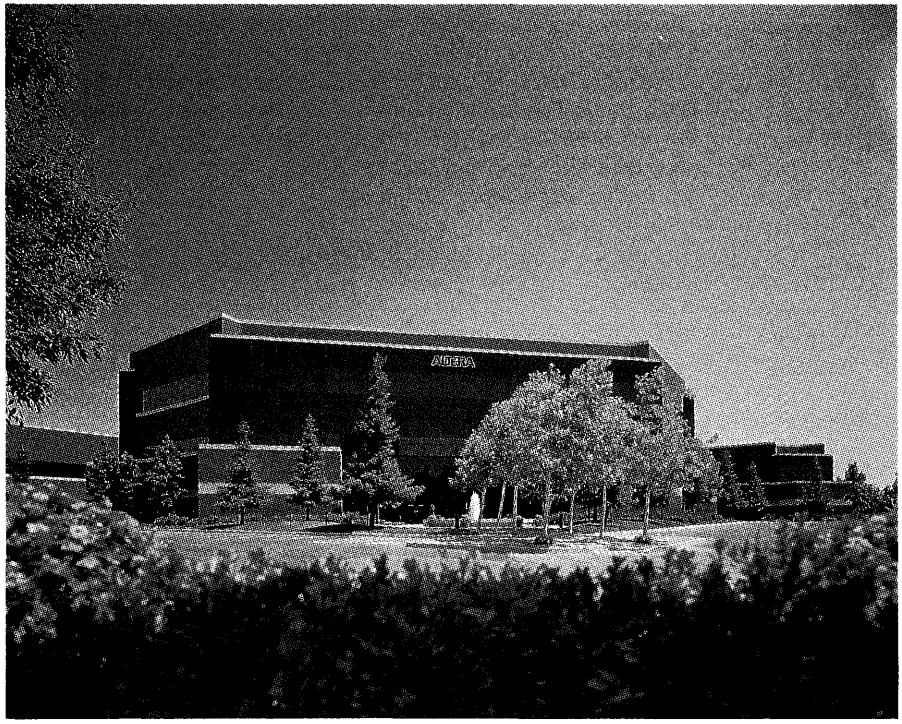
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MAX 7000

Programmable Logic Device Family

February 1993, ver. 1 Data Sheet

Features...

- High-performance, erasable CMOS devices based on second-generation Multiple Array MatriX (MAX) architecture
- Complete EPLD family with logic densities up to 10,000 available gates (5,000 usable gates). See Table 1.
- Fast, 10-ns pin-to-pin logic delays with up to 100-MHz true system performance (including interconnect)
- Programmable power-saver mode for 50% or more power reduction in each macrocell
- Programmable Security Bit for total protection of proprietary designs
- Configurable expander product-term distribution allowing up to 32 product terms in each macrocell
- 44 to 208 pins available in J-lead, pin-grid array (PGA), and quad flat pack (QFP) packages
- High pin-to-logic ratio with user-defined I/O options for pin-intensive applications such as 32-bit microprocessor interface logic
- Enhanced Programmable Interconnect Array (PIA) that provides a fast, fixed delay from any internal source to any destination in the device
- Advanced macrocell to efficiently place logic for optimum speed and density
- Programmable registers providing D, T, JK, and SR flipflops with individual Clear, Preset, Clock, and Clock Enable controls
- Independent clocking of all registers from array or global Clock signals
- 3.3-V operation provided by EPM7032V device

Table 1. MAX 7000 Device Features

Feature	EPM7032	EPM7032V	EPM7064	EPM7096	EPM7128	EPM7160	EPM7192	EPM7256
Available Gates	1,200	1,200	2,400	3,600	5,000	6,400	7,500	10,000
Usable Gates	600	600	1,200	1,800	2,500	3,200	3,750	5,000
Macrocells	32	32	64	96	128	160	192	256
Max. User I/O	36	36	68	76	100	104	124	164
t_{PD} (ns)	10	15	10	15	10	12	12	20
t_{ASU} (ns)	3	4	3	4	3	4	4	4
t_{CO} (ns)	5	8	5	10	5	6	6	12
f_{CNT} (MHz)	100	76.9	100	71.4	100	90.9	90.9	62.5

...and More Features

- Software design support featuring Altera's MAX+PLUS II development system on 386- or 486-based PCs and Sun SPARCstation or HP 9000 Series 700 workstations
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from other manufacturers
- EDIF, Verilog, VHDL netlist interfaces provide additional design entry and simulation support with popular CAE tools from vendors such as Cadence, Data I/O, Exemplar, Intergraph (formerly DAZIX), Mentor Graphics, OrCAD, Synopsys, and Viewlogic

General Description

The MAX 7000 family is a family of high-density, high-performance CMOS EPLDs based on Altera's second-generation MAX architecture. Fabricated on advanced 0.8-micron CMOS EEPROM and EPROM technologies, the MAX 7000 family provides 600 to 5,000 usable gates, pin-to-pin delays as low as 10 ns, and in-system speeds up to 100 MHz.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to MACH, pLSI, and FPGA devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 7000 EPLDs are also ideal for gate-array prototyping. MAX 7000 EPLDs are available in a wide range of packages, including ceramic or plastic J-lead chip carrier (JLCC/PLCC); ceramic, metal, plastic, or thin quad flat pack (CQFP/MQFP/PQFP/TQFP); and ceramic pin-grid array (PGA) packages. See Table 2.

Table 2. MAX 7000 Pin Count & Package Options *Note (1)*

Pin Count	EPM7032	EPM7032V	EPM7064	EPM7096	EPM7128	EPM7160	EPM7192	EPM7256
44	PLCC, PQFP, TQFP	PLCC, TQFP	–	–	–	–	–	–
68	–	–	PLCC	JLCC, PLCC	–	–	–	–
84	–	–	PLCC	JLCC, PLCC	PLCC	PLCC	–	–
100	–	–	PQFP	PQFP	PQFP	PQFP	–	–
160	–	–	–	–	PQFP	PQFP	PQFP, PGA	–
192	–	–	–	–	–	–	–	PGA
208	–	–	–	–	–	–	–	CQFP, MQFP

Note:
(1) Contact Altera for information on device package availability.

MAX 7000 EPLDs use CMOS EEPROM or EPROM cells to implement logic functions within the device. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. EPLDs can be reprogrammed for quick and efficient iterations during design development and debug cycles. Each EEPROM-based device is guaranteed for 100 program and erase cycles. Each EPROM-based device is guaranteed for 25 program and erase cycles.

MAX 7000 EPLDs contain from 32 to 256 macrocells that are combined into groups called Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides D, T, JK, or SR operation with independent programmable Clock, Clock Enable, Clear, and Preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remainder runs at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay.

The MAX 7000 EPLD family is supported by Altera's MAX+PLUS II development system, a single integrated package that offers schematic, text, and waveform design entry; compilation and logic synthesis; simulation; and programming software. MAX+PLUS II provides EDIF, VHDL, and Verilog netlist interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based CAE tools. The system runs on 386- and 486-based PCs or Sun SPARCstations and HP 9000 Series 700 workstations.

Functional Description

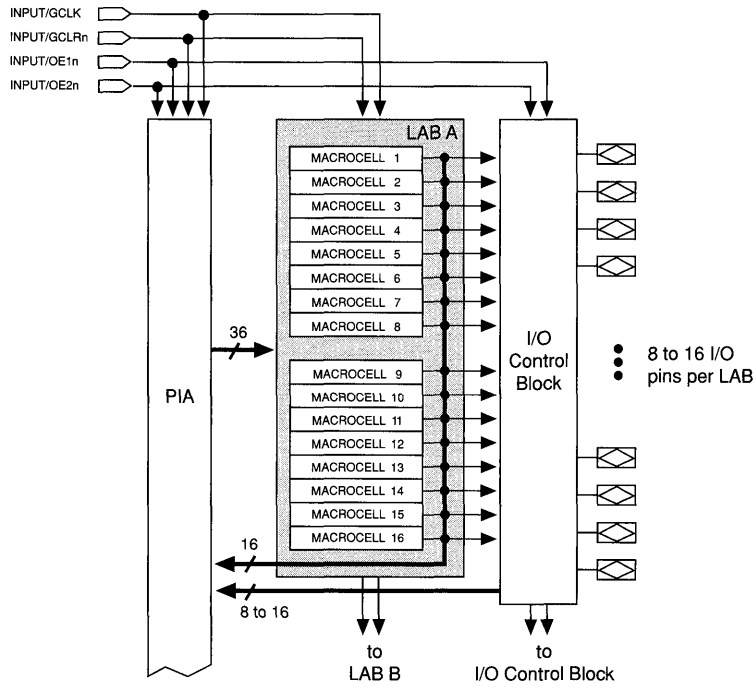
The MAX 7000 architecture includes the following elements:

- Logic Array Blocks
- Macrocells
- Expander product terms (shared and parallel)
- Programmable Interconnect Array
- I/O control blocks

In addition to these basic elements, the MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (Clock, Clear, and two Output Enable signals) for each macrocell and I/O pin. Figure 1 shows a portion of the MAX 7000 architecture.

Figure 1. MAX 7000 Architecture

This illustration shows a portion of the MAX 7000 architecture, including the Programmable Interconnect Array (PIA), a Logic Array Block (LAB), macrocells, and the I/O control block.



Logic Array Blocks

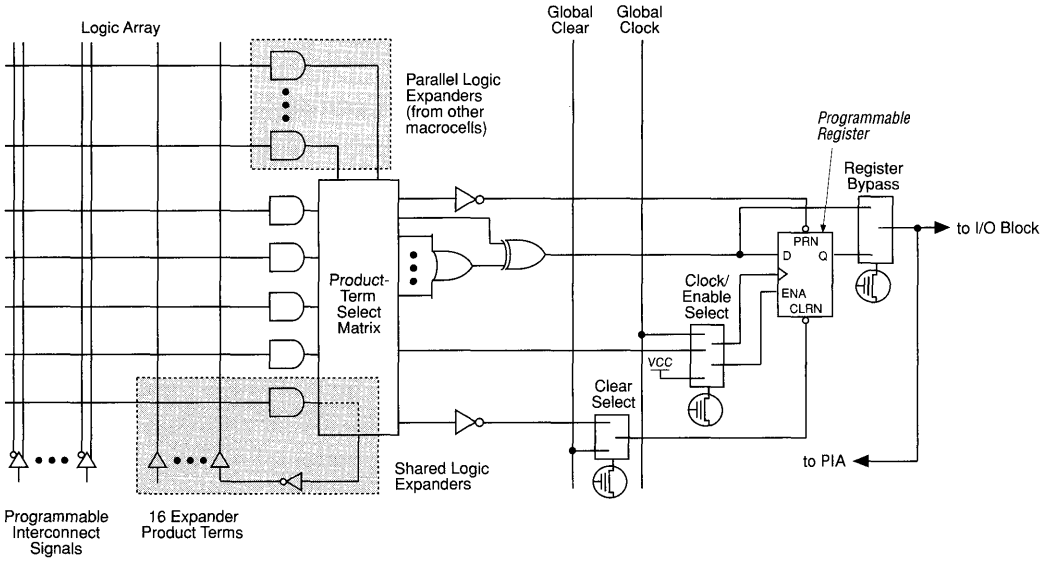
MAX 7000 architecture is based on the concept of linking small, high-performance, flexible logic array modules called Logic Array Blocks (LABs). Multiple LABs are linked together via the Programmable Interconnect Array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells. All inputs to each LAB, except the global control signals, are fed by 36 signals from the PIA.

Macrocells

The MAX 7000 macrocell, shown in Figure 2, can be individually configured for both sequential and combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

5 Ands and 5 ors

Figure 2. MAX 7000 Macrocell



Combinatorial logic is implemented in the logic array, which contains five product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register Clear, Preset, Clock, and Clock Enable control functions. One product term per macrocell can be inverted and directly fed back into the logic array. This "shareable" product term can be connected to any other product term within the LAB. Based on the logic requirements of the design, MAX+PLUS II automatically optimizes product-term allocation.

In registered functions, each macrocell flipflop can be individually programmed for D, T, JK, or SR operation with programmable Clock control. If necessary, the flipflop can be bypassed for combinatorial operation. During design entry, the user specifies the desired flipflop type and MAX+PLUS II selects the most efficient flipflop operation for each registered function to minimize the resources needed by the design.

Three clocking modes are available for each programmable register:

- A register can be clocked by the dedicated global Clock pin (GCLK). In this mode, the flipflop is positive-edge-triggered, and offers the fastest Clock-to-output performance.
- A register can be clocked by an array Clock implemented with a product term. In this mode, the flipflop can be configured for positive- or negative-edge-triggered operation. Array Clocks allow any signal source within the device or gated logic functions to clock the flipflop.
- A register can be clocked by a global Clock pin and enabled by a product term. The register is enabled when the its Clock Enable (ENA) input is high. Each flipflop can be activated individually while taking advantage of the fast Clock-to-output delay of the global Clock pin.

Each register also supports asynchronous Preset and Clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the register is designed for active-low Preset and Clear, active-high control is provided when the signal is inverted within the logic array. In addition, each register Clear function can be individually driven by the active-low dedicated global Clear pin (GCLRn).

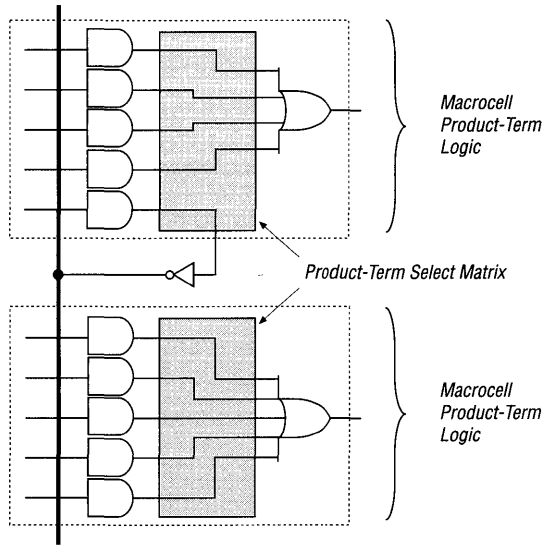
Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Instead of using another macrocell to supply the needed logic resources, the MAX 7000 architecture offers both shared and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Each LAB has up to 16 shareable expanders, which can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shareable expanders can also be cross-coupled to build additional buried flipflops, latches, or input registers. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



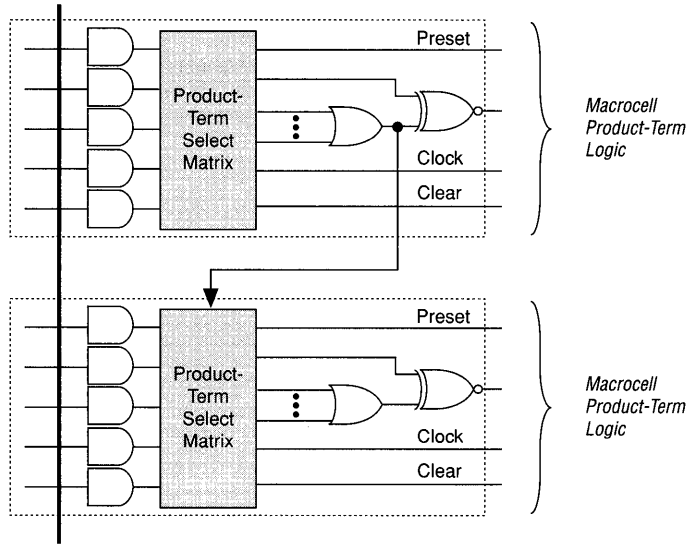
Parallel expanders are unused product terms from macrocells in the LAB. The product-term select matrix can allocate parallel expanders to any neighboring macrocell to implement fast, complex logic functions. With parallel expanders, up to 20 product terms can directly feed the macrocell OR logic—5 product terms from the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can automatically route a set of 1 to 5 parallel expanders to the necessary macrocells. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within the LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders; the highest-numbered macrocells can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. Parallel Logic Expanders

These unused product terms in a macrocell can be allocated to a neighboring macrocell.

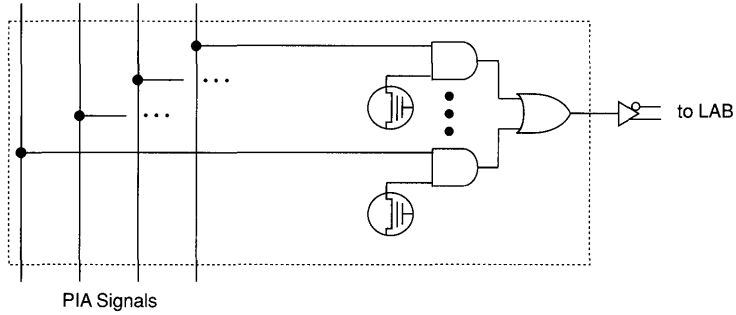


Programmable Interconnect Array

Logic is routed between LABs on the Programmable Interconnect Array (PIA). This global bus is a programmable path that routes any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pin feedbacks, and macrocell feedbacks feed the PIA and route across the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EPROM or EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals, and makes timing performance easy to predict.

Figure 5. PIA Routing

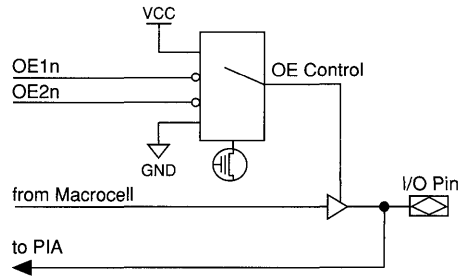


I/O Control Blocks

The I/O control block, shown in Figure 6, allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is controlled by one of two global active-low Output Enable pins (OE1n and OE2n) or directly connected to GND or VCC. When the tri-state buffer control is connected to GND, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to VCC, the output is enabled.

MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Figure 6. I/O Control Block



Programmable Speed/Power Control

The MAX 7000 family offers a power-saver mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, since most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 EPLD for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters.

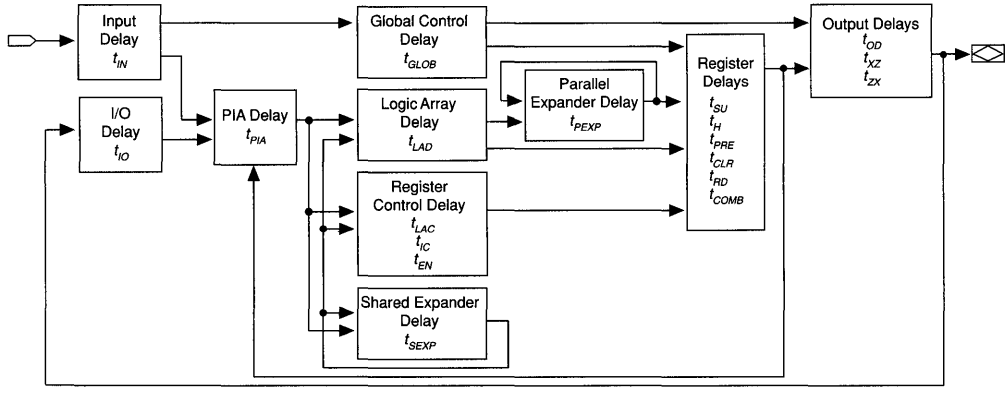
Design Security

All MAX 7000 EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM or EEPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when an EPLD is erased.

Timing Model

MAX 7000 EPLD timing can be analyzed with MAX+PLUS II software, with a variety of popular industry-standard CAE simulators and timing analyzers, or with the timing model shown in Figure 7. MAX 7000 devices have fixed internal delays that allow the user to determine the worst-case timing for any design. MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 7. Timing Model



Timing information can be calculated with the timing model and parameters for a particular EPLD. External timing parameters are derived from the sum of internal parameters and represent pin-to-pin timing delays. Figure 8 shows the internal timing relationship for internal and external delay parameters. Timing can also be calculated in a timing simulation or timing analysis with MAX+PLUS II or with other industry-standard CAE tools.

Figure 8. Switching Waveforms (Part 1 of 2)

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

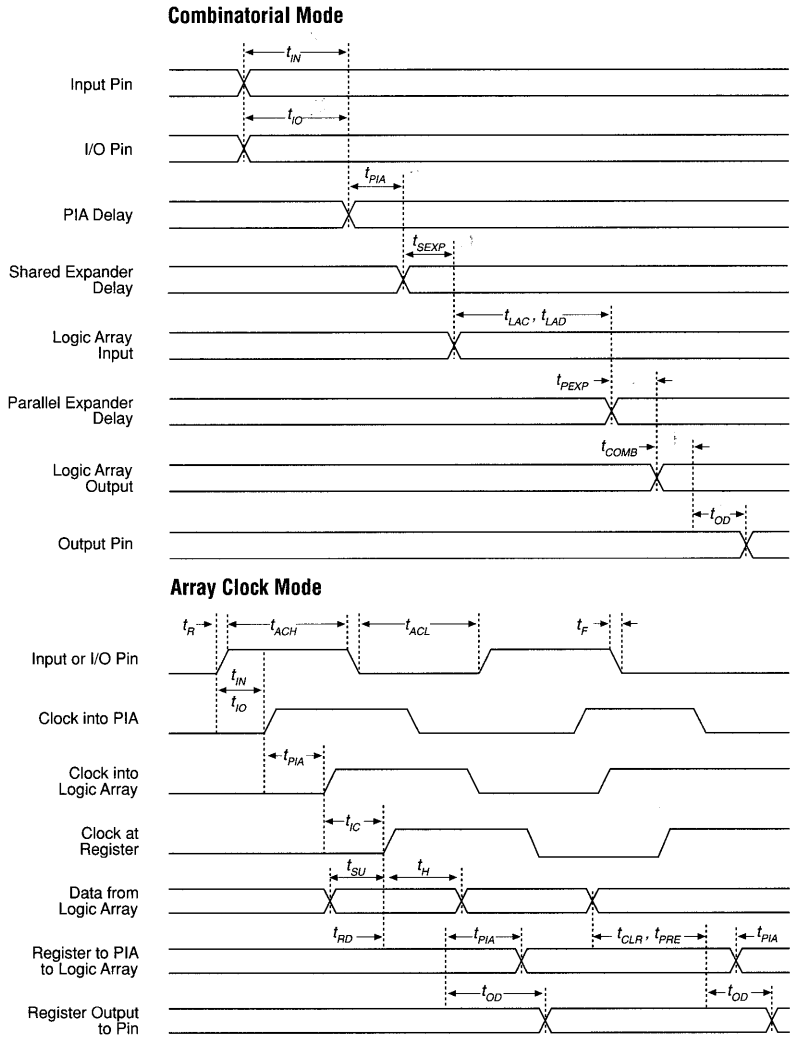
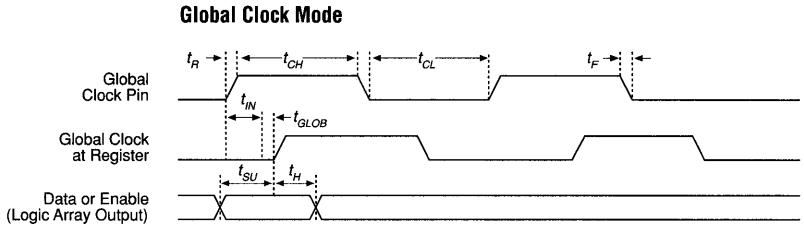


Figure 8. Switching Waveforms (Part 2 of 2)



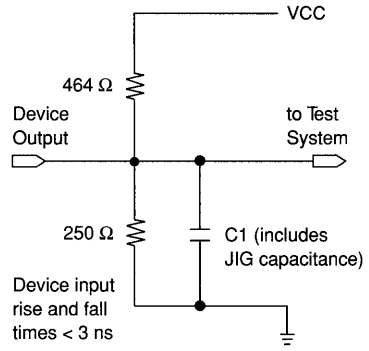
Generic Testing

MAX 7000 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EEPROM or EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under the conditions shown in Figure 9.

Test patterns can be used and then erased during early stages of the production flow. This facility to use application-independent, general-purpose tests, called generic testing, is unique among user-configurable logic devices.

Figure 9. MAX 7000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be perfomed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



MAX+PLUS II Development System

MAX 7000 EPLDs are supported by the MAX+PLUS II development system, a completely integrated environment for design entry, compilation, verification, and programming. MAX+PLUS II software is available for 386- and 486-based PCs, as well as Sun SPARCstation and HP 9000 Series 700 workstations. All platforms include more than 300 74-series macrofunctions and the Altera Hardware Description Language (AHDL), which supports state machine, Boolean equation, conditional logic, and truth table entry methods. MAX+PLUS II also provides highly automated compilation, automatic multi-device partitioning, timing simulation and analysis, automatic error location, device programming and verification,

and a comprehensive on-line help system. In addition, MAX+PLUS II imports and exports industry-standard EDIF 2 0 0 netlist files for a convenient interface to industry-standard PC- and workstation-based CAE tools from vendors such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic. MAX+PLUS II also exports Verilog or VHDL netlist files to support simulation with the Cadence Verilog-XL simulator or various VHDL simulators. For further details about MAX+PLUS II and other CAE tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and *CAE Software Support* in this data book.

Device Programming

All MAX 7000 EPLDs can be programmed on 386- or 486-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU supports open- and short-circuit testing, and performs continuity checking to ensure adequate electrical contact between the adapter and the device.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 EPLD with the results of simulation.

Data I/O and other programming hardware manufacturers also provide programming support for Altera devices. See *Programming Hardware Manufacturers* in this data book for more information.

QFP Carrier & Development Socket

MAX 7000 devices in 100-plus pin QFP packages are shipped in special plastic carriers to protect the fragile QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress. For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet* in this data book.

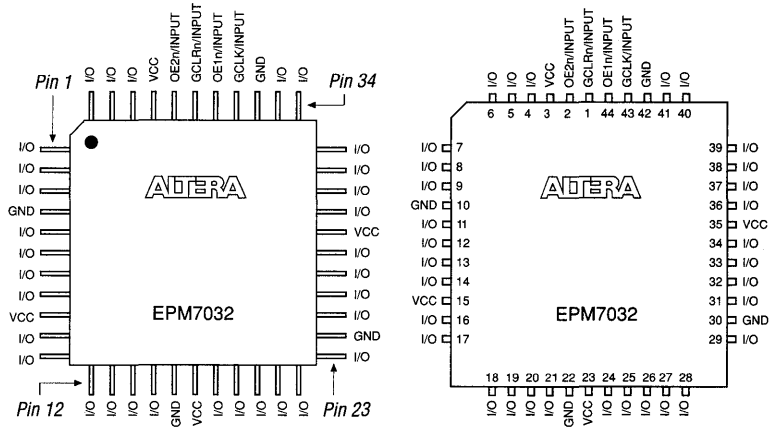
Notes:

Features

- High-performance, erasable CMOS EPLD based on second-generation Multiple Array MatriX (MAX) architecture
  - 600 usable gates
  - Combinatorial speeds with t_{PD} = 10 ns
  - Clock frequencies up to 111 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 36 inputs or 32 outputs
- 32 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing 32 product terms in a single macrocell
- Available in 44-pin EIAJ-standard plastic quad flat pack (PQFP), thin quad flat pack (TQFP), and 44-pin plastic J-lead chip carrier (PLCC) reprogrammable packages (see Figure 10)

Figure 10. EPM7032 Package Pin-Out Diagrams

Package outlines not drawn to scale.



General Description

The Altera EPM7032 is a high-performance, high-density CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 11. Fabricated on a 0.8-micron EEPROM technology, the EPM7032 provides in-system speeds of 111 MHz and propagation delays of 10 ns. The EPM7032 architecture supports 100% TTL emulation and allows the integration of SSI, MSI, and custom logic functions. It can replace multiple 20- and 24-pin PLDs. The EPM7032 can accommodate designs with up to 36 inputs or 32 outputs.

Figure 11. EPM7032 Block Diagram

Pin numbers are for the PLCC package. Pin numbers in parentheses are for the PQFP package.

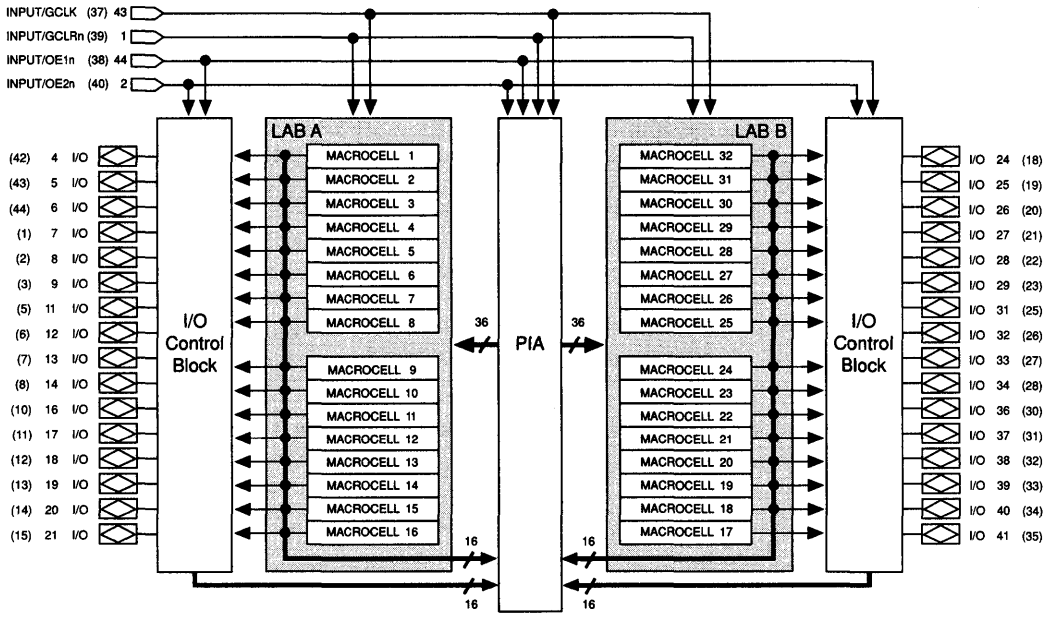


Figure 12 shows the output drive characteristics of EPM7032 I/O pins.

Figure 12. Typical EPM7032 Output Drive Characteristics

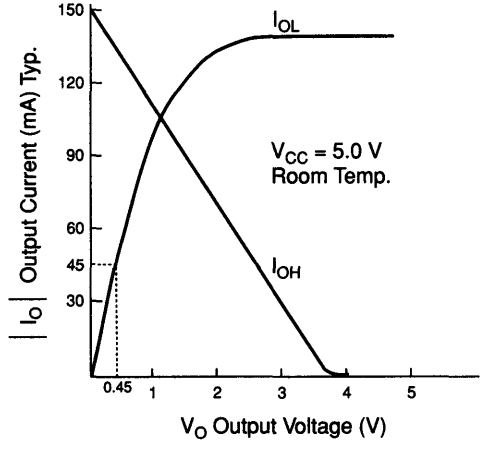


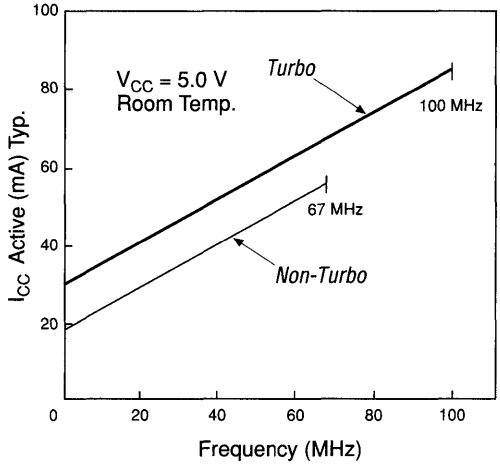
Figure 13 shows typical supply current versus frequency for the EPM7032.

Figure 13. EPM7032 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (0.9 \times MC_{TON}) + (0.55 \times MC_{TOFF}) + [(0.018 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings See *Note (1)* and *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load *Note (5)*		24	35	mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *Note (5)*		30	40	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM7032-1		EPM7032-2		EPM7032-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		12		15	ns
t_{PD2}	I/O input to non-registered output			10		12		15	ns
t_{SU}	Global clock setup time		8		10		11		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5		6		8	ns
t_{CH}	Global clock high time		4		4		5		ns
t_{CL}	Global clock low time		4		4		5		ns
t_{ASU}	Array clock setup time		3		4		4		ns
t_{AH}	Array clock hold time		3		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		12		15	ns
t_{ACH}	Array clock high time		4		5		6		ns
t_{ACL}	Array clock low time		4		5		6		ns
t_{CNT}	Minimum global clock period			10		11		13	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	100		90.9		76.9		MHz
t_{ACNT}	Minimum array clock period			10		11		13	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	100		90.9		76.9		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	125		125		100		MHz

Internal Timing Parameters			EPM7032-1		EPM7032-2		EPM7032-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			1		2		2	ns
t_{IO}	I/O input pad and buffer delay			1		2		2	ns
t_{SEXP}	Shared expander delay			5		7		8	ns
t_{PEXP}	Parallel expander delay			0.8		1		1	ns
t_{LAD}	Logic array delay			5		5		6	ns
t_{LAC}	Logic control array delay			5		5		6	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2		3		4	ns
t_{ZX}	Output buffer enable delay			5		6		6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		6		6	ns
t_{SU}	Register setup time		3		4		4		ns
t_{H}	Register hold time		3		4		4		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			5		5		6	ns
t_{EN}	Register enable time			5		5		6	ns
t_{GLOB}	Global control delay			1		0		1	ns
t_{PRE}	Register preset time			3		3		4	ns
t_{CLR}	Register clear time			3		3		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		1		2	ns
t_{LPA}	Low power adder	*Note (8)*		5		7		9	ns

Notes to tables:

(1) Operation outside the absolute maximum ratings may permanently damage the device. Extended operation at absolute maximum ratings may impair device reliability.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.

(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.

(5) Measured with a device programmed as a 16-bit loadable, enabled, up/down counter in each LAB at 0° C.

(6) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

(7) The f_{MAX} values represent the highest frequency for pipelined data.

(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7032-1, EPM7032-2, EPM7032-3
Industrial	(–40° C to 85° C)	EPM7032-2, EPM7032-3
Military	(–55° C to 125° C)	Consult factory

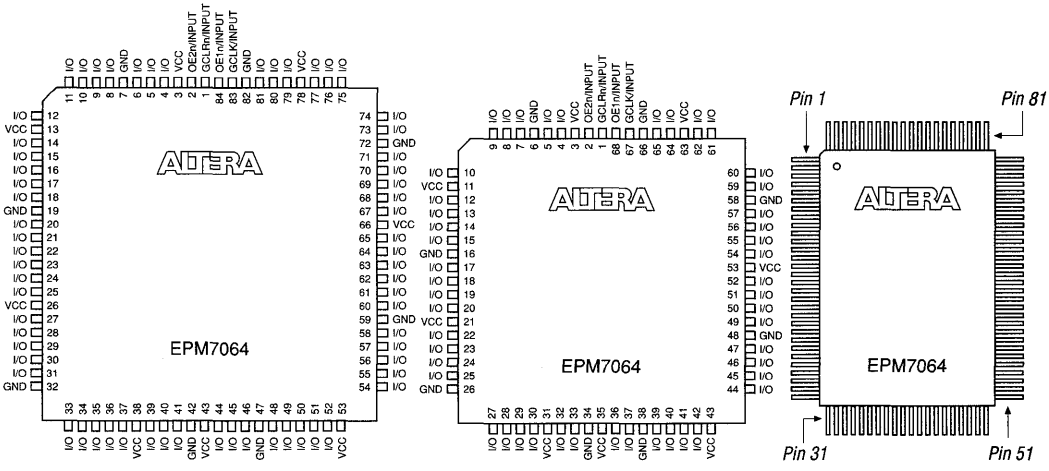
Features

Preliminary Information

- High-performance, erasable CMOS EPLD based on second-generation Multiple Array MatriX (MAX) architecture
  - 1,200 usable gates
  - Combinatorial speeds with t_{PD} = 10 ns
  - Clock frequencies up to 100 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 68 inputs or 64 outputs
- 64 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing 32 product terms in a single macrocell
- Available in 68- or 84-pin plastic J-lead chip carrier (PLCC) and 100-pin EIAJ-standard plastic quad flat pack (PQFP) packages (see Figure 14)

Figure 14. EPM7064 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 3 and 4 in this data sheet for pin-out information.



84-Pin J-Lead 68-Pin J-Lead 100-Pin QFP

General Description

The Altera EPM7064 is a high-performance, high-density CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 15. Fabricated on a 0.8-micron EEPROM technology, the EPM7064 provides in-system speeds of 100 MHz and propagation delays of 10 ns. The EPM7064 architecture supports 100% TTL emulation and allows the integration of SSI, MSI, and custom logic functions. It can replace multiple 20- and 24-pin PLDs and can accomodate designs with up to 68 inputs or 64 outputs.

Figure 15. EPM7064 Block Diagram

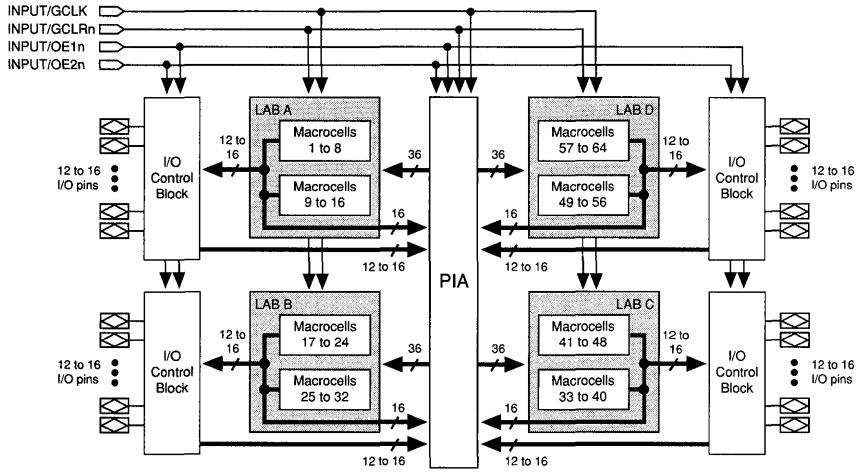
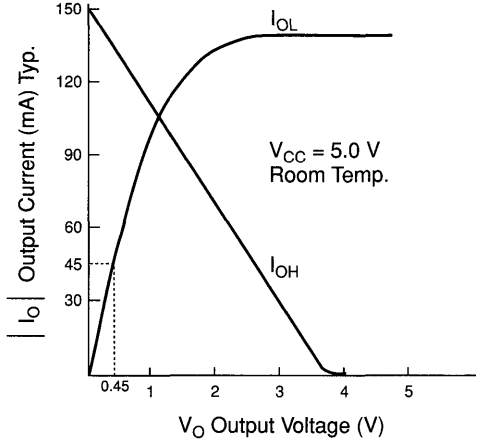


Figure 16 shows the output drive characteristics of EPM7064 I/O pins.

Figure 16. Typical EPM7064 Output Drive Characteristics



Absolute Maximum Ratings

See *Note (1)* and *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load *Note (5)*		40		mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *Note (5)*		45		mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM7064-1		EPM7064-2		EPM7064-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		12		15	ns
t_{PD2}	I/O input to non-registered output			10		12		15	ns
t_{SU}	Global clock setup time		8		10		11		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5		6		8	ns
t_{CH}	Global clock high time		4		4		5		ns
t_{CL}	Global clock low time		4		4		5		ns
t_{ASU}	Array clock setup time		3		4		4		ns
t_{AH}	Array clock hold time		3		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		12		15	ns
t_{ACH}	Array clock high time		4		5		6		ns
t_{ACL}	Array clock low time		4		5		6		ns
t_{CNT}	Minimum global clock period			10		11		13	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	100		90.9		76.9		MHz
t_{ACNT}	Minimum array clock period			10		11		13	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	100		90.9		76.9		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	125		125		100		MHz

Internal Timing Parameters			EPM7064-1		EPM7064-2		EPM7064-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			1		2		2	ns
t_{IO}	I/O input pad and buffer delay			1		2		2	ns
t_{SEXP}	Shared expander delay			5		7		8	ns
t_{PEXP}	Parallel expander delay			0.8		1		1	ns
t_{LAD}	Logic array delay			5		5		6	ns
t_{LAC}	Logic control array delay			5		5		6	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2		3		4	ns
t_{ZX}	Output buffer enable delay			5		6		6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		6		6	ns
t_{SU}	Register setup time		3		4		4		ns
t_{H}	Register hold time		3		4		4		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			5		5		6	ns
t_{EN}	Register enable time			5		5		6	ns
t_{GLOB}	Global control delay			1		0		1	ns
t_{PRE}	Register preset time			3		3		4	ns
t_{CLR}	Register clear time			3		3		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		1		2	ns
t_{LPA}	Low power adder	*Note (8)*		5		7		9	ns

Notes to tables:

(1) Operation outside the absolute maximum ratings may permanently damage the device. Extended operation at absolute maximum ratings may impair device reliability.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a device programmed as a 16-bit loadable, enabled, up/down counter in each LAB at 0° C.
(6) Capacitance measured at 25° C. Sample tested only. The OE1n pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	Consult factory
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Pin-Out Information

Tables 3 and 4 provide pin-out information for the EPM7064 packages.

Table 3. EPM7064 Dedicated Pin-Outs

Dedicated Pin	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
GCLK	67	83	89
GCLRn	1	1	91
OE1n	68	84	90
OE2n	2	2	92
GND	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCC	3, 11, 21, 31, 35, 43, 53, 63	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93
No Connect (N.C.)			1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80

Table 4. EPM7064 Pin-Outs

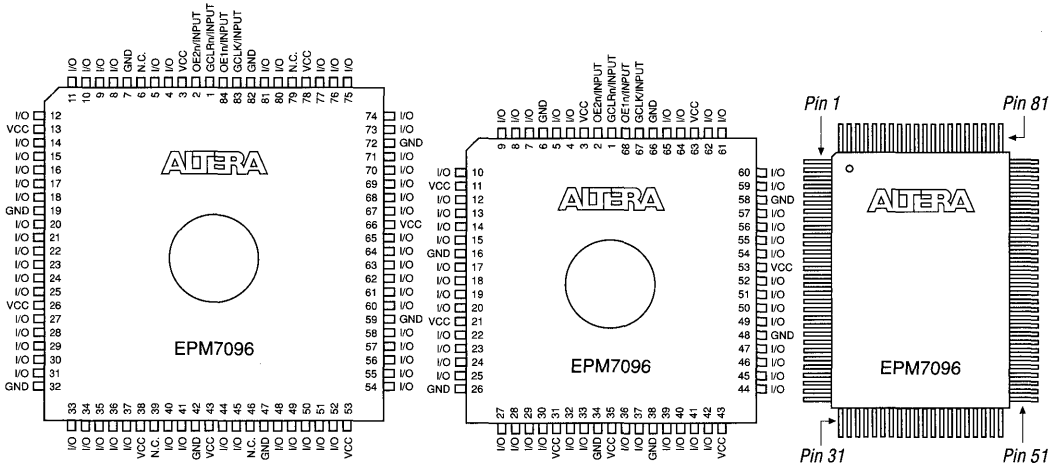
MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
1	A	18	22	16	17	B	33	41	39
2	A	–	21	15	18	B	–	40	38
3	A	17	20	14	19	B	32	39	37
4	A	15	18	12	20	B	30	37	35
5	A	14	17	11	21	B	29	36	34
6	A	13	16	10	22	B	28	35	33
7	A	–	15	8	23	B	–	34	32
8	A	12	14	6	24	B	27	33	31
9	A	10	12	4	25	B	25	31	27
10	A	–	11	3	26	B	–	30	25
11	A	9	10	100	27	B	24	29	23
12	A	8	9	99	28	B	23	28	22
13	A	7	8	98	29	B	22	27	21
14	A	5	6	96	30	B	20	25	19
15	A	–	5	95	31	B	–	24	18
16	A	4	4	94	32	B	19	23	17
33	C	36	44	42	49	D	51	63	65
34	C	–	45	43	50	D	–	64	66
35	C	37	46	44	51	D	52	65	67
36	C	39	48	46	52	D	54	67	69
37	C	40	49	47	53	D	55	68	70
38	C	41	50	48	54	D	56	69	71
39	C	–	51	49	55	D	–	70	73
40	C	42	52	50	56	D	57	71	75
41	C	44	54	54	57	D	59	73	77
42	C	–	55	56	58	D	–	74	78
43	C	45	56	58	59	D	60	75	81
44	C	46	57	59	60	D	61	76	82
45	C	47	58	60	61	D	62	77	83
46	C	49	60	62	62	D	64	79	85
47	C	–	61	63	63	D	–	80	86
48	C	50	62	64	64	D	65	81	87

Features

- High-density, erasable CMOS EPLD based on second-generation Multiple Array MatriX (MAX) architecture
  - 1,800 usable gates
  - Combinatorial speeds with t_{PD} = 15 ns
  - Clock frequencies up to 71.4 MHz
- Advanced 0.8-micron CMOS EPROM technology
- Programmable I/O architecture providing up to 76 inputs or 72 outputs
- 96 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in 68- and 84-pin windowed ceramic J-lead chip carrier (JLCC), one-time programmable (OTP) plastic J-lead chip carrier (PLCC), and 100-pin EIAJ-standard plastic quad flat pack (PQFP) packages (see Figure 17)

Figure 17. EPM7096 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 5 and 6 in this data sheet for pin-out information.



84-Pin J-Lead 68-Pin J-Lead 100-Pin QFP

General Description

The Altera EPM7096 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 18. Fabricated on a 0.8-micron EPROM technology, the EPM7096 provides 1,800 usable gates, in-system speeds of 71.4 MHz, and propagation delays of 15 ns. The EPM7096 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs,

and 22V10s to MACH devices and FPGAs. The EPM7096 can accommodate designs with up to 76 inputs or 72 outputs.

Figure 18. EPM7096 Block Diagram

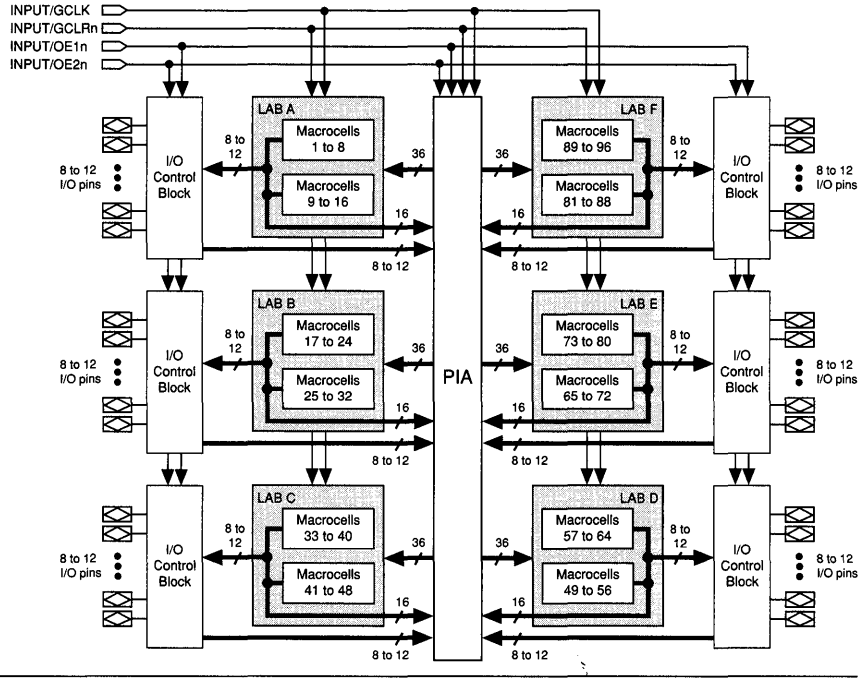


Figure 19 shows the output drive characteristics of EPM7096 I/O pins.

Figure 19. EPM7096 Output Drive Characteristics

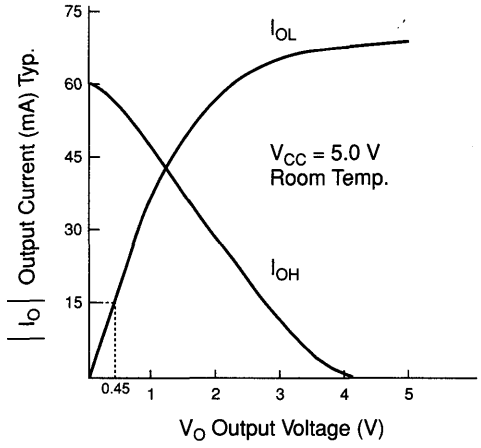


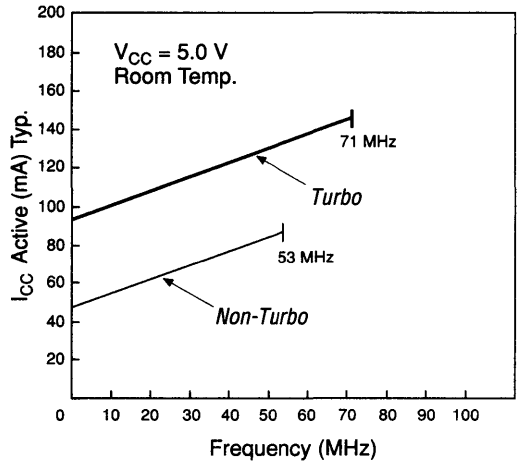
Figure 20 shows typical supply current versus frequency for the EPM7096.

Figure 20. EPM7096 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (0.9 \times MC_{TON}) + (0.49 \times MC_{TOFF}) + [(0.01 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings See *Note (1)* and *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load *Note (5)*		50	80	mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *Note (5)*		55	90	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM7096-2		EPM7096-3		EPM7096		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20		25	ns
t_{PD2}	I/O input to non-registered output			15		20		25	ns
t_{SU}	Global clock setup time		9		12		15		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		10		12		15	ns
t_{CH}	Global clock high time		5		6		8		ns
t_{CL}	Global clock low time		5		6		8		ns
t_{ASU}	Array clock setup time		4		5		6		ns
t_{AH}	Array clock hold time		4		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		20		25	ns
t_{ACH}	Array clock high time		6		8		12.5		ns
t_{ACL}	Array clock low time		6		8		12.5		ns
t_{CNT}	Minimum global clock period			14		16		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	71.4		62.5		50		MHz
t_{ACNT}	Minimum array clock period			14		16		25	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	71.4		62.5		40		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	100		83.3		62.5		MHz

Internal Timing Parameters			EPM7096-2		EPM7096-3		EPM7096		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			1		3		4	ns
t_{IO}	I/O input pad and buffer delay			1		3		4	ns
t_{SEXP}	Shared expander delay			7		8		10	ns
t_{PEXP}	Parallel expander delay			2		2		3	ns
t_{LAD}	Logic array delay			7		8		10	ns
t_{LAC}	Logic control array delay			7		8		10	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		5		6	ns
t_{ZX}	Output buffer enable delay			6		9		12	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		9		12	ns
t_{SU}	Register setup time		4		4		5		ns
t_{H}	Register hold time		4		5		6		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			7		8		10	ns
t_{EN}	Register enable time			7		8		10	ns
t_{GLOB}	Global control delay			4		3		4	ns
t_{PRE}	Register preset time			4		4		4	ns
t_{CLR}	Register clear time			4		4		4	ns
t_{PIA}	Prog. Interconnect Array delay			2		3		4	ns
t_{LPA}	Low power adder	*Note (8)*		6		7		8	ns

Notes to tables:

(1) Operation outside the absolute maximum ratings may permanently damage the device. Extended operation at absolute maximum ratings may impair device reliability.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as a 16-bit, loadable, enabled, up/down counter in each LAB at 0° C.
(6) Capacitance measured at 25° C. Sample-tested only. The OE1n pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7096, EPM7096-2, EPM7096-3
Industrial	(–40° C to 85° C)	EPM7096-3
Military	(–55° C to 125° C)	Consult factory

Pin-Out Information

Tables 5 and 6 provide pin-out information for the EPM7096 packages.

Table 5. EPM7096 Dedicated Pin-Outs

Dedicated Pin	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
GCLK	67	83	89
GCLRn	1	1	91
OE1n	68	84	90
OE2n	2	2	92
GND	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCC	3, 11, 21, 31, 35, 43, 53, 63	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93
No Connect (N.C.)		6, 39, 46, 79	9, 24, 37, 44, 57, 72, 85, 96

Table 6. EPM7096 Pin-Outs (Part 1 of 2)

MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
1	A	13	16	8	17	B	23	28	23
2	A	–	–	–	18	B	–	–	–
3	A	–	15	7	19	B	22	27	22
4	A	12	14	6	20	B	–	–	21
5	A	–	–	4	21	B	20	25	19
6	A	10	12	3	22	B	–	24	18
7	A	–	–	–	23	B	–	–	–
8	A	9	11	2	24	B	19	23	17
9	A	8	10	1	25	B	18	22	16
10	A	–	–	–	26	B	–	–	–
11	A	–	9	100	27	B	17	21	15
12	A	7	8	99	28	B	–	20	14
13	A	–	–	98	29	B	15	18	12
14	A	5	5	95	30	B	–	–	11
15	A	–	–	–	31	B	–	–	–
16	A	4	4	94	32	B	14	17	10
33	C	33	41	39	49	D	36	44	42
34	C	–	–	–	50	D	–	–	–
35	C	32	40	38	51	D	37	45	43
36	C	–	–	35	52	D	–	–	46
37	C	30	37	34	53	D	39	48	47
38	C	–	36	33	54	D	–	49	48
39	C	–	–	–	55	D	–	–	–
40	C	29	35	32	56	D	40	50	49
41	C	28	34	31	57	D	41	51	50
42	C	–	–	–	58	D	–	–	–
43	C	27	33	30	59	D	42	52	51
44	C	–	–	29	60	D	–	–	52
45	C	25	31	27	61	D	44	54	54
46	C	–	30	26	62	D	–	55	55
47	C	–	–	–	63	D	–	–	–
48	C	24	29	25	64	D	45	56	56

Table 6. EPM7096 Pin-Outs (Part 2 of 2)

MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
65	E	46	57	58	81	F	56	69	73
66	E	–	–	–	82	F	–	–	–
67	E	47	58	59	83	F	–	70	74
68	E	–	–	60	84	F	57	71	75
69	E	49	60	62	85	F	–	–	77
70	E	–	61	63	86	F	59	73	78
71	E	–	–	–	87	F	–	–	–
72	E	50	62	64	88	F	60	74	79
73	E	51	63	65	89	F	61	75	80
74	E	–	–	–	90	F	–	–	–
75	E	52	64	66	91	F	–	76	81
76	E	–	65	67	92	F	62	77	82
77	E	54	67	69	93	F	–	–	83
78	E	–	–	70	94	F	64	80	86
79	E	–	–	–	95	F	–	–	–
80	E	55	68	71	96	F	65	81	87

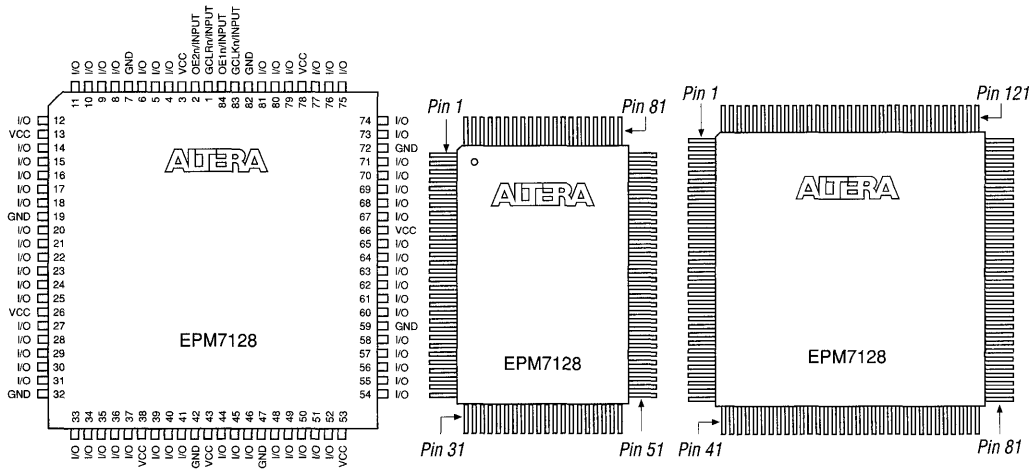
Features

Preliminary Information

- High-density CMOS EPLD based on second-generation Multiple Array MatriX (MAX) architecture
  - 2,500 usable gates
  - Combinatorial speeds with t_{PD} = 10 ns
  - Clock frequencies up to 100 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 100 inputs or 96 outputs
- 128 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in 84-pin plastic J-lead chip carrier (PLCC) and 160-pin plastic quad flat pack (PQFP) packages (see Figure 21). A 100-pin PQFP package is under development.

Figure 21. EPM7128 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 7 and 8 in this data sheet for pin-out information.



84-Pin J-Lead 100-Pin QFP 160-Pin QFP

General Description

The Altera EPM7128 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 22. Fabricated on a 0.8-micron EEPROM technology, the EPM7128 provides 2,500 usable gates, in-system speeds of 100 MHz, and propagation delays of 10 ns. The EPM7128 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 128 macrocells, the EPM7128 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs,

and 22V10s. With its high performance and density, the EPM7128 provides FPGA density with PAL performance. The high density and high I/O pin count make the EPM7128 appropriate for prototyping gate arrays. The EPM7128 can also accommodate both logic- and I/O-intensive designs.

Figure 22. EPM7128 Block Diagram

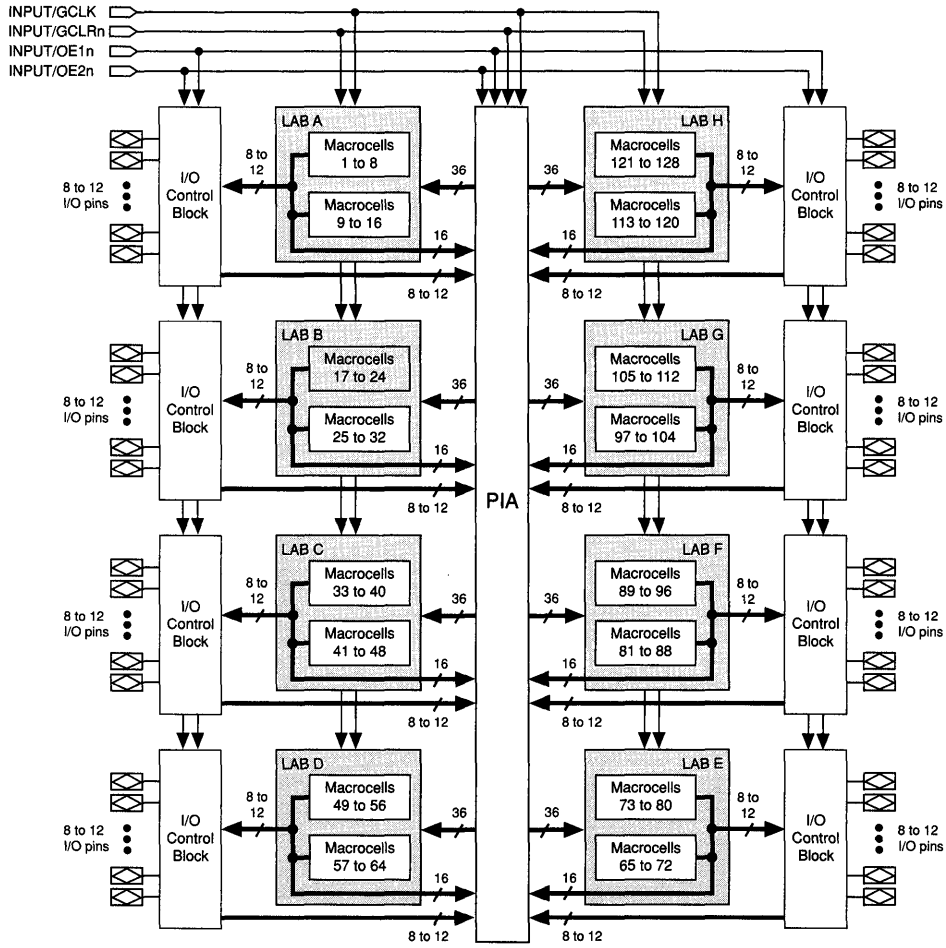


Figure 23 shows the output drive characteristics of EPM7128 I/O pins.

Figure 23. EPM7128 Output Drive Characteristics

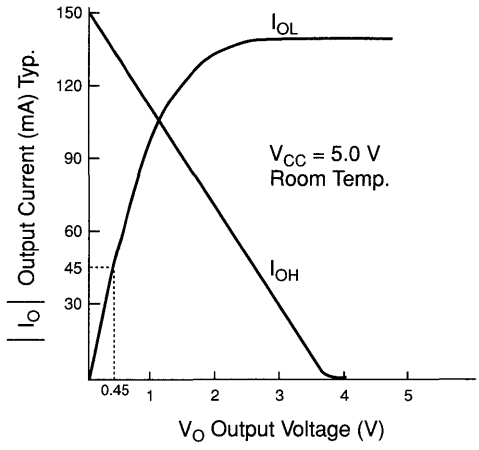


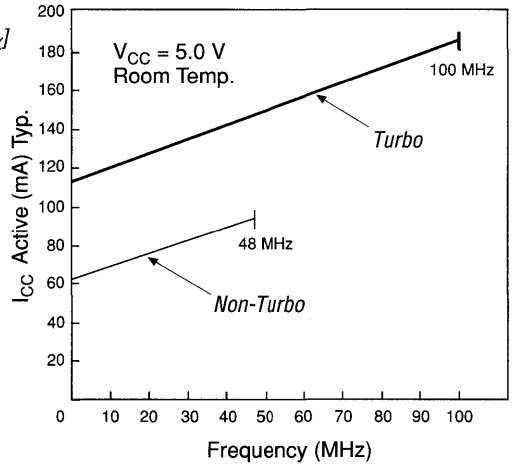
Figure 24 shows typical supply current versus frequency for the EPM7128.

Figure 24. EPM7128 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (0.91 \times MC_{TON}) + (0.48 \times MC_{TOFF}) + [(0.0053 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Rating

See *Note (1)* and *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load *Note (5)*		90		mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *Note (5)*		100		mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM7128-1		EPM7128-2		EPM7128-3		EPM7128-4		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-reg. output	C1 = 35 pF		10		12		15		20	ns
t_{PD2}	I/O input to non-reg. output			10		12		15		20	ns
t_{SU}	Global clock setup time		8		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5		6		8		12	ns
t_{CH}	Global clock high time		4		4		5		6		ns
t_{CL}	Global clock low time		4		4		5		6		ns
t_{ASU}	Array clock setup time		3		4		4		5		ns
t_{AH}	Array clock hold time		3		4		4		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		12		15		20	ns
t_{ACH}	Array clock high time		4		5		6		8		ns
t_{ACL}	Array clock low time		4		5		6		8		ns
t_{CNT}	Minimum global clock period			10		11		13		16	ns
f_{CNT}	Max. int. global clock freq.	*Note (5)*	100		90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			10		11		13		16	ns
f_{ACNT}	Max. int. array clock freq.	*Note (5)*	100		90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	125		125		100		83.3		MHz

Internal Timing Parameters			EPM7128-1		EPM7128-2		EPM7128-3		EPM7128-4		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad & buffer delay			1		2		2		3	ns
t_{IO}	I/O input pad & buffer delay			1		2		2		3	ns
t_{SEXP}	Shared expander delay			5		7		8		9	ns
t_{PEXP}	Parallel expander delay			0.8		1		1		2	ns
t_{LAD}	Logic array delay			5		5		6		8	ns
t_{LAC}	Logic control array delay			5		5		6		8	ns
t_{OD}	Output buffer & pad delay	C1 = 35 pF		2		3		4		5	ns
t_{ZX}	Output buffer enable delay			5		6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		6		6		9	ns
t_{SU}	Register setup time		3		4		4		4		ns
t_{H}	Register hold time		3		4		4		5		ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{IC}	Array clock delay			5		5		6		8	ns
t_{EN}	Register enable time			5		5		6		8	ns
t_{GLOB}	Global control delay			1		0		1		3	ns
t_{PRE}	Register preset time			3		3		4		4	ns
t_{CLR}	Register clear time			3		3		4		4	ns
t_{PIA}	Prog. Interconn. Array delay			1		1		2		3	ns
t_{LPA}	Low power adder	*Note (8)*		11		12		13		15	ns

Notes to tables:

(1) Operation outside the absolute maximum ratings may permanently damage the device. Extended operation at absolute maximum ratings may impair device reliability.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as a 16-bit loadable, enabled up/down counter in each LAB at 0° C.
(6) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 25 pF.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{EN}, t_{SEXP} and t_{ACL} parameters for macrocells running in low-power mode.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7128-2, EPM7128-3, EPM7128-4
Industrial	(–40° C to 85° C)	EPM7128-4
Military	(–55° C to 125° C)	Consult factory

Pin-Out Information

Tables 7 and 8 provide pin-out information for the EPM7128 packages.

Table 7. EPM7128 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
GCLK	83	89	139
GCLRn	1	92	141
OE1n	84	90	140
OE2n	2	91	142
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCC	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93	8, 26, 55, 61, 79, 104, 133, 143
No Connect (N.C.)			1, 2, 3, 4, 5, 6, 7, 34, 35, 36, 37, 38, 39, 40, 44, 45, 46, 47, 74, 75, 76, 77, 81, 82, 83, 84, 85, 86, 87, 114, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157

Table 8. EPM7128 Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
1	A	–	4	160	17	B	22	16	21
2	A	–	–	–	18	B	–	–	–
3	A	12	3	159	19	B	21	15	20
4	A	–	–	158	20	B	–	–	19
5	A	11	2	153	21	B	20	14	18
6	A	10	1	152	22	B	–	12	16
7	A	–	–	–	23	B	–	–	–
8	A	9	100	151	24	B	18	11	15
9	A	–	99	150	25	B	17	10	14
10	A	–	–	–	26	B	–	–	–
11	A	8	98	149	27	B	16	9	13
12	A	–	–	147	28	B	–	–	12
13	A	6	96	146	29	B	15	8	11
14	A	5	95	145	30	B	–	7	10
15	A	–	–	–	31	B	–	–	–
16	A	4	94	144	32	B	14	6	9
33	C	–	27	41	49	D	41	39	59
34	C	–	–	–	50	D	–	–	–
35	C	31	26	33	51	D	40	38	58
36	C	–	–	32	52	D	–	–	57
37	C	30	25	31	53	D	39	37	56
38	C	29	24	30	54	D	–	35	54
39	C	–	–	–	55	D	–	–	–
40	C	28	23	29	56	D	37	34	53
41	C	–	22	28	57	D	36	33	52
42	C	–	–	–	58	D	–	–	–
43	C	27	21	27	59	D	35	32	51
44	C	–	–	25	60	D	–	–	50
45	C	25	19	24	61	D	34	31	49
46	C	24	18	23	62	D	–	30	48
47	C	–	–	–	63	D	–	–	–
48	C	23	17	22	64	D	33	27	43

Table 8. EPM7128 Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
65	E	44	42	62	81	F	–	54	80
66	E	–	–	–	82	F	–	–	–
67	E	45	43	63	83	F	54	55	88
68	E	–	–	64	84	F	–	–	89
69	E	46	44	65	85	F	55	56	90
70	E	–	46	67	86	F	56	57	91
71	E	–	–	–	87	F	–	–	–
72	E	48	47	68	88	F	57	58	92
73	E	49	48	69	89	F	–	59	93
74	E	–	–	–	90	F	–	–	–
75	E	50	49	70	91	F	58	60	94
76	E	–	–	71	92	F	–	–	96
77	E	51	50	72	93	F	60	62	97
78	E	–	51	73	94	F	61	63	98
79	E	–	–	–	95	F	–	–	–
80	E	52	52	78	96	F	62	64	99
97	G	63	65	100	113	H	–	77	121
98	G	–	–	–	114	H	–	–	–
99	G	64	66	101	115	H	73	78	122
100	G	–	–	102	116	H	–	–	123
101	G	65	67	103	117	H	74	79	128
102	G	–	69	105	118	H	75	80	129
103	G	–	–	–	119	H	–	–	–
104	G	67	70	106	120	H	76	81	130
105	G	68	71	107	121	H	–	82	131
106	G	–	–	–	122	H	–	–	–
107	G	69	72	108	123	H	77	83	132
108	G	–	–	109	124	H	–	–	134
109	G	70	73	110	125	H	79	85	135
110	G	–	74	111	126	H	80	86	136
111	G	–	–	–	127	H	–	–	–
112	G	71	75	112	128	H	81	87	137

EPM7160 EPLD

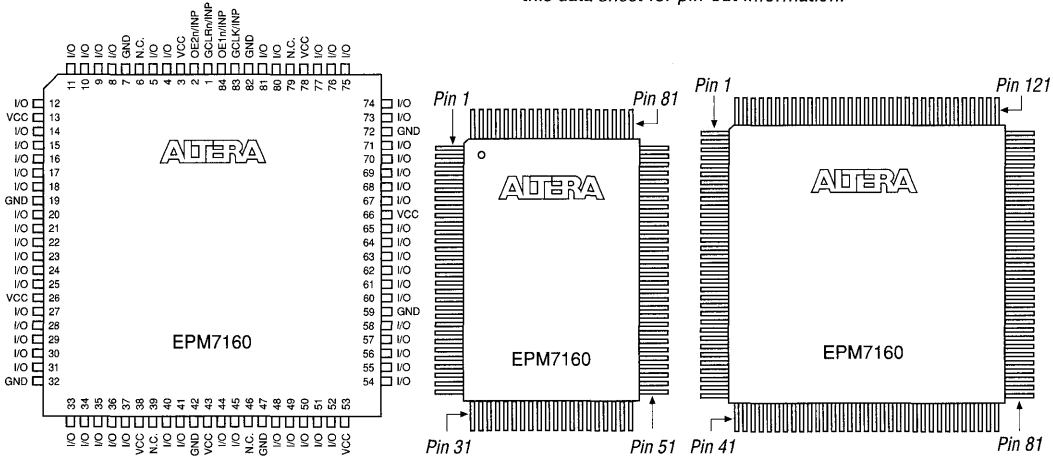
Features

Preliminary Information

- High-density, erasable CMOS EPLD based on second-generation Multiple Array MatriX (MAX) architecture
  - 3,200 usable gates
  - Combinatorial speeds with t_{PD} = 12 ns
  - Clock frequencies up to 90.9 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 104 inputs or 100 outputs
- 160 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in 84-pin plastic J-lead chip carrier (PLCC) or 100- and 160-pin plastic quad flat pack (PQFP) packages (see Figure 25)

Figure 25. EPM7160 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 9 and 10 in this data sheet for pin-out information.



General Description

The Altera EPM7160 is a high-density, high-performance CMOS device based on Altera's second-generation MAX architecture. See Figure 26. Fabricated on a 0.8-micron EEPROM technology, the EPM7160 provides 3,200 usable gates, in-system speeds of 90.9 MHz, and propagation delays of 12 ns. The EPM7160 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 160 macrocells, the EPM7160 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs, and 22V10s. With its high performance and density, the EPM7160 provides FPGA density with PAL performance. The high density and high I/O pin

count also make the EPM7160 appropriate for prototyping gate arrays. The EPM7160 can accommodate both logic- and I/O-intensive designs.

Figure 26. EPM7160 Block Diagram

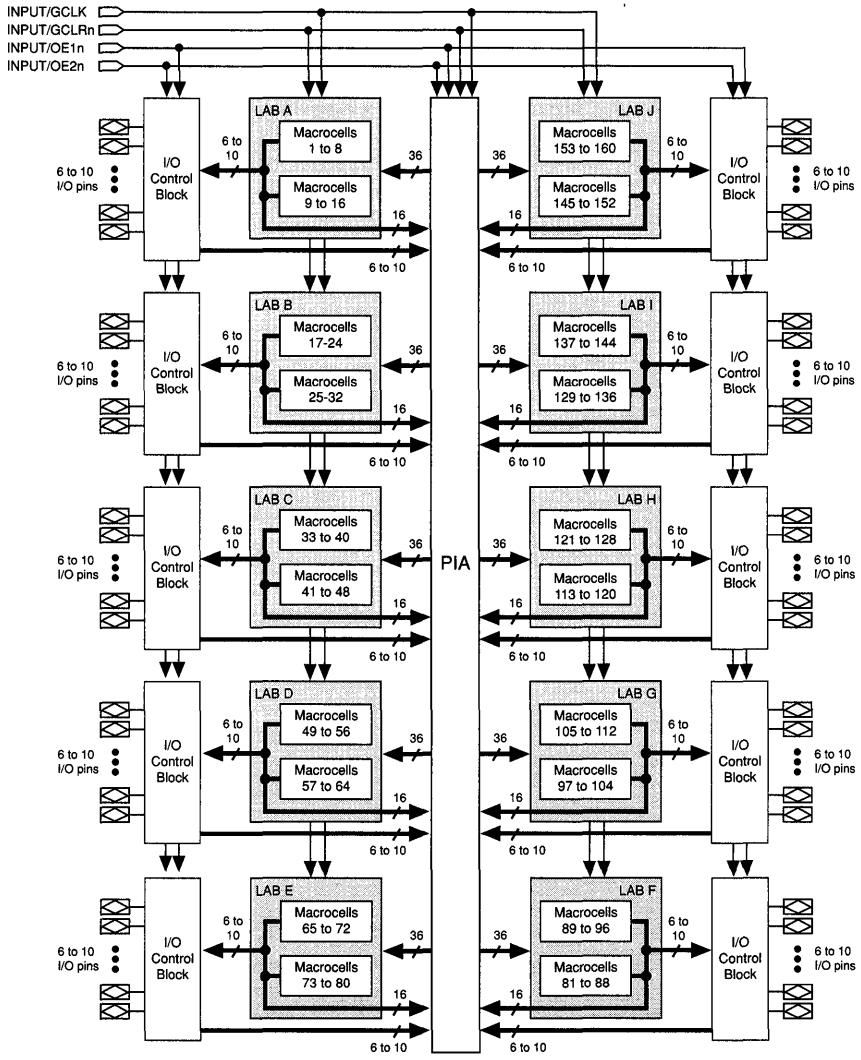


Figure 27 shows the output drive characteristics of EPM7160 I/O pins.

Figure 27. EPM7160 Output Drive Characteristics

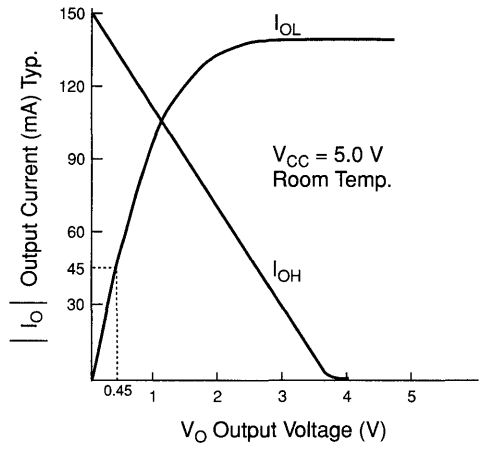


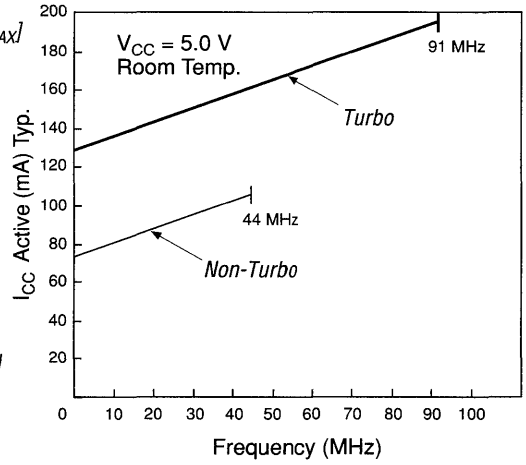
Figure 28 shows typical supply current versus frequency for the EPM7096.

Figure 28. EPM7160 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (0.82 \times MC_{TON}) + (0.43 \times MC_{TOFF}) + [(0.0046 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings

See *Note (1)* and *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load *Note (5)*		110		mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *Note (5)*		115		mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPM7160-1		EPM7160-2		EPM7160-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output			12		15		20	ns
t_{SU}	Global clock setup time		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		9		12	ns
t_{CH}	Global clock high time		4		5		6		ns
t_{CL}	Global clock low time		4		5		6		ns
t_{ASU}	Array clock setup time		4		5		5		ns
t_{AH}	Array clock hold time		4		5		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		15		20	ns
t_{ACH}	Array clock high time		5		6		8		ns
t_{ACL}	Array clock low time		5		6		8		ns
t_{CNT}	Minimum global clock period			11		13		15	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	90.9		76.9		66.6		MHz
t_{ACNT}	Minimum array clock period			11		13		15	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	90.9		76.9		66.6		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	125		100		83.3		MHz

Internal Timing Parameters			EPM7160-1		EPM7160-2		EPM7160-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		3		3	ns
t_{IO}	I/O input pad and buffer delay			2		3		3	ns
t_{SEXP}	Shared expander delay			7		8		9	ns
t_{PEXP}	Parallel expander delay			1		2		2	ns
t_{LAD}	Logic array delay			5		5		8	ns
t_{LAC}	Logic control array delay			5		5		8	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4		5	ns
t_{ZX}	Output buffer enable delay			6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		9	ns
t_{SU}	Register setup time		4		5		4		ns
t_{H}	Register hold time		4		5		5		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			5		5		8	ns
t_{EN}	Register enable time			5		5		8	ns
t_{GLOB}	Global control delay			0		1		3	ns
t_{PRE}	Register preset time			3		4		4	ns
t_{CLR}	Register clear time			3		4		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		2		3	ns
t_{LPA}	Low power adder	*Note (8)*		12		13		15	ns

Notes to tables:

(1) Operation outside the absolute maximum ratings may permanently damage the device. Extended operation at absolute maximum ratings may impair device reliability.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as a 16-bit loadable, enabled up/down counter in each LAB at 0° C.
(6) Capacitance measured at 25° C. Sample tested only. `OE1n` (high-voltage pin during programming) has a capacitance of 25 pF.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{EN}, t_{SEXP}, and t_{ACL} parameters for macrocells running in low-power mode.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7160-1, EPM7160-2, EPM7160-3
Industrial	(–40° C to 85° C)	EPM7160-3
Military	(–55° C to 125° C)	Consult factory

Pin-Out Information

Tables 9 and 10 provide pin-out information for the EPM7160 packages.

Table 9. EPM7160 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
GCLK	83	89	139
GCLRn	1	91	141
OE1n	84	90	140
OE2n	2	92	142
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCC	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93	8, 26, 55, 61, 79, 104, 133, 143
No Connect (N.C.)	6, 39, 46, 79		1, 2, 3, 4, 5, 6, 34, 35, 36, 37, 38, 39, 40, 45, 46, 47, 74, 75, 76, 81, 82, 83, 84, 85, 86, 87, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157

Table 10. EPM7160 Pin-Outs (Part 1 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
1	A	11	2	158	17	B	18	11	15
2	A	–	–	–	18	B	–	–	–
3	A	10	1	153	19	B	17	10	14
4	A	–	–	–	20	B	–	–	–
5	A	–	–	152	21	B	–	–	13
6	A	–	100	151	22	B	–	9	12
7	A	–	–	–	23	B	–	–	–
8	A	9	99	150	24	B	16	8	11
9	A	8	98	149	25	B	15	7	10
10	A	–	–	–	26	B	–	–	–
11	A	5	96	147	27	B	14	6	9
12	A	–	–	–	28	B	–	–	–
13	A	–	–	146	29	B	–	–	7
14	A	–	95	145	30	B	–	4	160
15	A	–	–	–	31	B	–	–	–
16	A	4	94	144	32	B	12	3	159
33	C	–	21	27	49	D	–	–	48
34	C	–	–	–	50	D	–	–	–
35	C	25	19	25	51	D	33	30	44
36	C	–	–	–	52	D	–	–	–
37	C	–	–	24	53	D	–	29	43
38	C	24	18	23	54	D	31	27	41
39	C	–	–	–	55	D	–	–	–
40	C	23	17	22	56	D	30	26	33
41	C	–	12	16	57	D	–	–	32
42	C	–	–	–	58	D	–	–	–
43	C	20	14	18	59	D	29	25	31
44	C	–	–	–	60	D	–	–	–
45	C	–	–	19	61	D	–	24	30
46	C	21	15	20	62	D	28	23	29
47	C	–	–	–	63	D	–	–	–
48	C	22	16	21	64	D	27	22	28

Table 10. EPM7160 Pin-Outs (Part 2 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
65	E	–	–	59	81	F	–	–	62
66	E	–	–	–	82	F	–	–	–
67	E	41	39	58	83	F	44	42	63
68	E	–	–	–	84	F	–	–	–
69	E	–	38	57	85	F	–	43	64
70	E	40	37	56	86	F	45	44	65
71	E	–	–	–	87	F	–	–	–
72	E	37	35	54	88	F	48	46	67
73	E	–	–	53	89	F	–	–	68
74	E	–	–	–	90	F	–	–	–
75	E	36	34	52	91	F	49	47	69
76	E	–	–	–	92	F	–	–	–
77	E	–	33	51	93	F	–	48	70
78	E	35	32	50	94	F	50	49	71
79	E	–	–	–	95	F	–	–	–
80	E	34	31	49	96	F	51	50	72
97	G	–	–	73	113	H	–	60	94
98	G	–	–	–	114	H	–	–	–
99	G	52	51	77	115	H	60	62	96
100	G	–	–	–	116	H	–	–	–
101	G	–	52	78	117	H	–	–	97
102	G	54	54	80	118	H	61	63	98
103	G	–	–	–	119	H	–	–	–
104	G	55	55	88	120	H	62	64	99
105	G	–	–	89	121	H	–	69	105
106	G	–	–	–	122	H	–	–	–
107	G	56	56	90	123	H	65	67	103
108	G	–	–	–	124	H	–	–	–
109	G	–	57	91	125	H	–	–	102
110	G	57	58	92	126	H	64	66	101
111	G	–	–	–	127	H	–	–	–
112	G	58	59	93	128	H	63	65	100

Table 10. EPM7160 Pin-Outs (Part 3 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
129	I	67	70	106	145	J	74	79	123
130	I	–	–	–	146	J	–	–	–
131	I	68	71	107	147	J	75	80	128
132	I	–	–	–	148	J	–	–	–
133	I	–	–	108	149	J	–	–	129
134	I	–	72	109	150	J	–	81	130
135	I	–	–	–	151	J	–	–	–
136	I	69	73	110	152	J	76	82	131
137	I	70	74	111	153	J	77	83	132
138	I	–	–	–	154	J	–	–	–
139	I	71	75	112	155	J	80	85	134
140	I	–	–	–	156	J	–	–	–
141	I	–	–	114	157	J	–	–	135
142	I	–	77	121	158	J	–	86	136
143	I	–	–	–	159	J	–	–	–
144	I	73	78	122	160	J	81	87	137

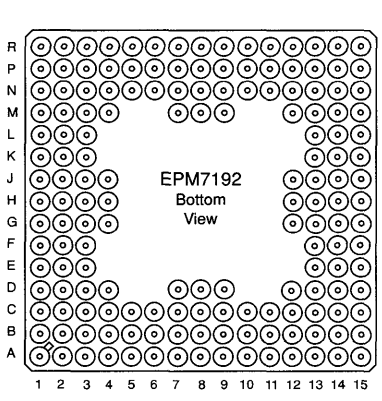
Notes:

Features

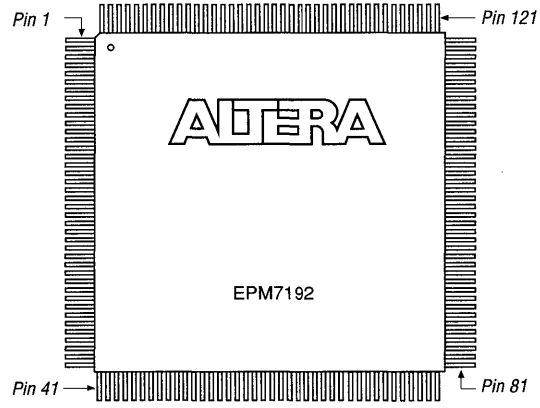
- High-density, erasable CMOS EPLD based on second-generation Multiple Array MatriX (MAX) architecture
  - 3,750 usable gates
  - Combinatorial speeds with t_{PD} = 12 ns
  - Clock frequencies up to 90.9 MHz
- Advanced 0.8-micron CMOS EPROM technology
- Programmable I/O architecture providing up to 124 inputs or 120 outputs
- 192 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in 160-pin pin-grid array (PGA) and plastic quad flat pack (PQFP) packages (see Figure 29)

Figure 29. EPM7192 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 11 and 12 in this data sheet for pin-out information.



160-Pin PGA



160-Pin QFP

General Description

The Altera EPM7192 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 30. Fabricated on a 0.8-micron EEPROM technology, the EPM7192 provides 3,750 usable gates, in-system speeds of 90.9 MHz and propagation delays of 12 ns. The EPM7192 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 192 macrocells, the EPM7192 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs, and 22V10s. The high density and high I/O pin count make the EPM7192

appropriate for prototyping gate arrays. The EPM7192 can accommodate both logic- and I/O-intensive designs.

Figure 30. EPM7192 Block Diagram

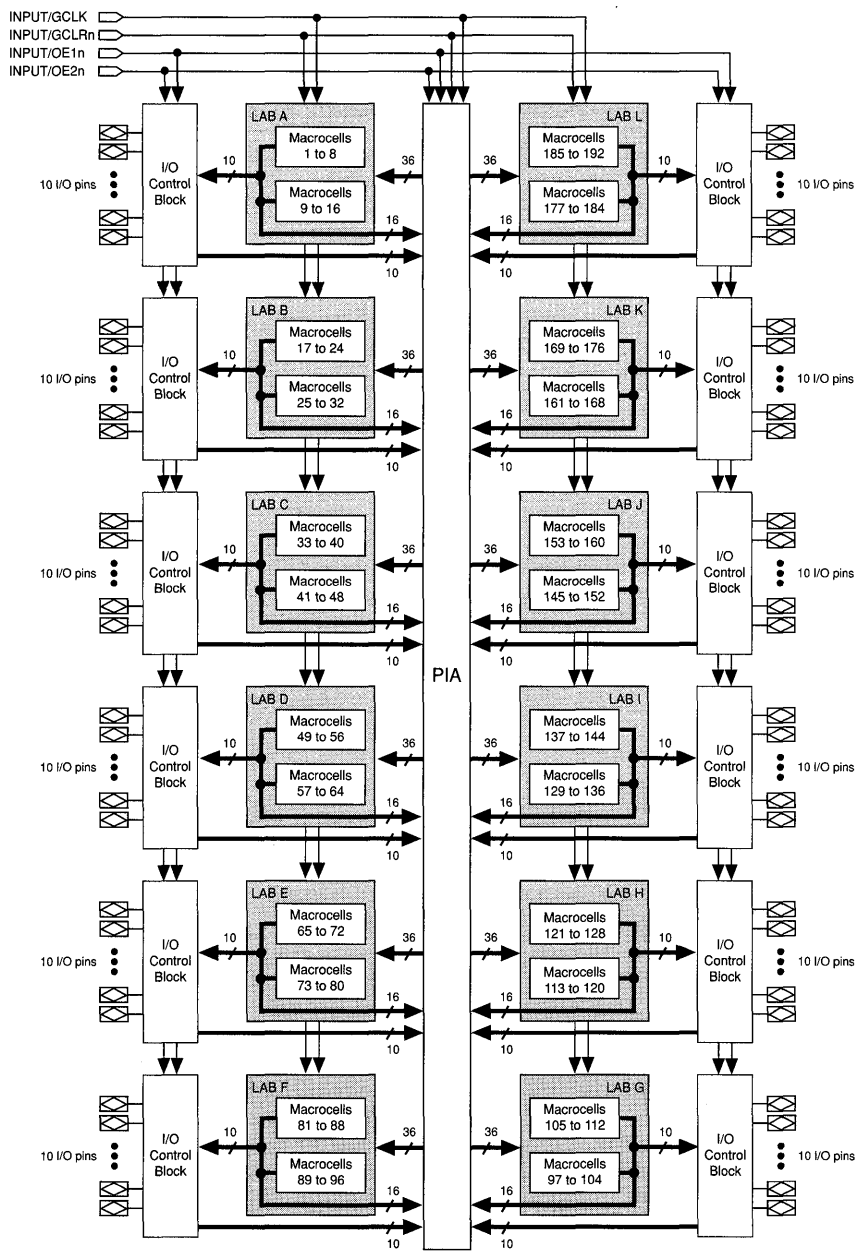


Figure 31 shows the output drive characteristics of EPM7192 I/O pins.

Figure 31. EPM7192 Output Drive Characteristics

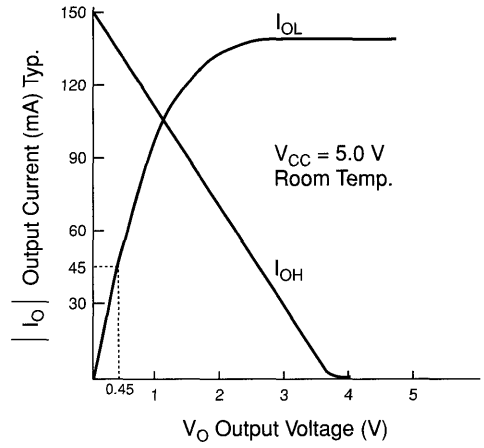


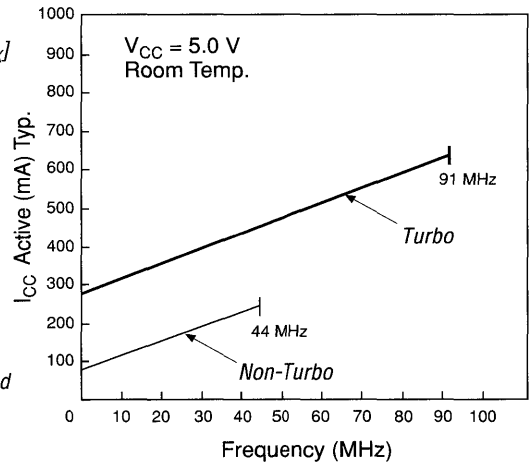
Figure 32 shows typical supply current versus frequency for the EPM7192.

Figure 32. EPM7192 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (1.4 \times MC_{TON}) + (0.48 \times MC_{TOFF}) + [(0.019 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings

See *Note (1)* and *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load *Note (5)*		130		mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *Note (5)*		135		mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM7192-1		EPM7192-2		EPM7192-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output			12		15		20	ns
t_{SU}	Global clock setup time		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		9		12	ns
t_{CH}	Global clock high time		4		5		6		ns
t_{CL}	Global clock low time		4		5		6		ns
t_{ASU}	Array clock setup time		4		5		5		ns
t_{AH}	Array clock hold time		4		5		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		15		20	ns
t_{ACH}	Array clock high time		5		6		8		ns
t_{ACL}	Array clock low time		5		6		8		ns
t_{CNT}	Minimum global clock period			11		13		16	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			11		13		16	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	125		100		83.3		MHz

Internal Timing Parameters			EPM7192-1		EPM7192-2		EPM7192-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		3		3	ns
t_{IO}	I/O input pad and buffer delay			2		3		3	ns
t_{SEXP}	Shared expander delay			7		8		9	ns
t_{PEXP}	Parallel expander delay			1		2		2	ns
t_{LAD}	Logic array delay			5		5		8	ns
t_{LAC}	Logic control array delay			5		5		8	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4		5	ns
t_{ZX}	Output buffer enable delay			6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		9	ns
t_{SU}	Register setup time		4		5		4		ns
t_{H}	Register hold time		4		5		5		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			5		5		8	ns
t_{EN}	Register enable time			5		5		8	ns
t_{GLOB}	Global control delay			0		1		3	ns
t_{PRE}	Register preset time			3		4		4	ns
t_{CLR}	Register clear time			3		4		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		2		3	ns
t_{LPA}	Low power adder	*Note (8)*		12		13		15	ns

Notes to tables:

(1) Operation outside the absolute maximum ratings may permanently damage the device. Extended operation at absolute maximum ratings may impair device reliability.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.

(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.

(5) Measured with a device programmed as a 16-bit loadable, enabled, up/down counter in each LAB at 0° C.

(6) Capacitance measured at 25° C. Sample-tested only. The OE1n pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

(7) The f_{MAX} values represent the highest frequency for pipelined data.

(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7192-1, EPM7192-2, EPM7192-3
Industrial	(–40° C to 85° C)	EPM7192-3
Military	(–55° C to 125° C)	Consult factory

Pin-Out Information

Tables 11 and 12 provide pin-out information for the EPM7192 packages.

Table 11. EPM7192 Dedicated Pin-Outs

Dedicated Pin	160-Pin PGA	160-Pin QFP
GCLK	M8	139
GCLRn	N8	141
OE1n	P8	140
OE2n	R8	142
GND	C4, C6, C11, D7, D9, D13, G4, H12, J4, M7, M9, M13, N4, N11	3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148
VCC	C5, C7, C9, C10, C12, D3, G12, H4, J12, M3, N5, N7, N9, N12	10, 25,40,55, 56, 65, 74, 89, 103, 118, 133, 137, 144, 155
No Connect (N.C.)	A1, A2, A14, A15, R1, R2, R14, R15	1, 11, 39,54, 67, 82, 110, 120

Table 12. EPM7192 Pin-Outs (Part 1 of 2)

MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP
1	A	M12	156	17	B	L14	8	33	C	H14	21
2	A	–	–	18	B	–	–	34	C	–	–
3	A	P11	154	19	B	M14	7	35	C	J13	20
4	A	–	–	20	B	–	–	36	C	–	–
5	A	P12	153	21	B	M15	6	37	C	H15	19
6	A	P10	152	22	B	N14	5	38	C	J15	17
7	A	–	–	23	B	–	–	39	C	–	–
8	A	R12	151	24	B	N15	4	40	C	J14	16
9	A	N10	150	25	B	P15	2	41	C	K15	15
10	A	–	–	26	B	–	–	42	C	–	–
11	A	R11	149	27	B	N13	160	43	C	K13	14
12	A	–	–	28	B	–	–	44	C	–	–
13	A	R10	147	29	B	P14	159	45	C	L15	13
14	A	P9	146	30	B	P13	158	46	C	K14	12
15	A	–	–	31	B	–	–	47	C	–	–
16	A	R9	145	32	B	R13	157	48	C	L13	9
49	D	D15	33	65	E	B12	45	81	F	D8	60
50	D	–	–	66	E	–	–	82	F	–	–
51	D	E15	31	67	E	B13	44	83	F	A9	59
52	D	–	–	68	E	–	–	84	F	–	–
53	D	E14	30	69	E	C13	43	85	F	C8	58
54	D	F15	29	70	E	B14	42	86	F	B9	53
55	D	–	–	71	E	–	–	87	F	–	–
56	D	F13	28	72	E	C14	41	88	F	A10	52
57	D	G14	27	73	E	D12	38	89	F	B10	51
58	D	–	–	74	E	–	–	90	F	–	–
59	D	F14	26	75	E	B15	37	91	F	A11	50
60	D	–	–	76	E	–	–	92	F	–	–
61	D	G13	24	77	E	D14	36	93	F	B11	49
62	D	G15	23	78	E	C15	35	94	F	A12	48
63	D	–	–	79	E	–	–	95	F	–	–
64	D	H13	22	80	E	E13	34	96	F	A13	46

Table 12. EPM7192 Pin-Outs (Part 2 of 2)

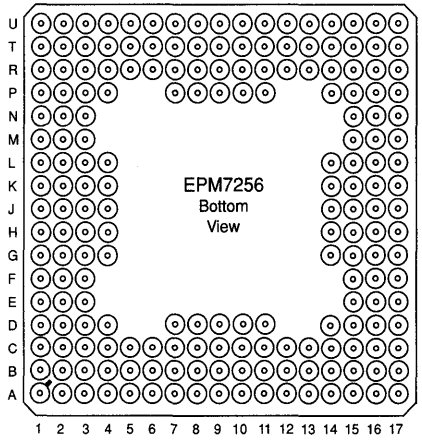
MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP
97	G	A8	61	113	H	A3	76	129	I	E3	88
98	G	–	–	114	H	–	–	130	I	–	–
99	G	B8	62	115	H	B4	77	131	I	F3	90
100	G	–	–	116	H	–	–	132	I	–	–
101	G	A7	63	117	H	B3	78	133	I	E2	91
102	G	A6	68	118	H	C3	79	134	I	F2	92
103	G	–	–	119	H	–	–	135	I	–	–
104	G	B7	69	120	H	B2	80	136	I	E1	93
105	G	A5	70	121	H	B1	83	137	I	G3	94
106	G	–	–	122	H	–	–	138	I	–	–
107	G	B6	71	123	H	C2	84	139	I	F1	95
108	G	–	–	124	H	–	–	140	I	–	–
109	G	A4	72	125	H	C1	85	141	I	G1	97
110	G	B5	73	126	H	D2	86	142	I	G2	98
111	G	–	–	127	H	–	–	143	I	–	–
112	G	D4	75	128	H	D1	87	144	I	H1	99
145	J	H2	100	161	K	L2	113	177	L	R3	125
146	J	–	–	162	K	–	–	178	L	–	–
147	J	J1	101	163	K	N1	114	179	L	R4	127
148	J	–	–	164	K	–	–	180	L	–	–
149	J	H3	102	165	K	L3	115	181	L	M4	128
150	J	J3	104	166	K	P1	116	182	L	R5	129
151	J	–	–	167	K	–	–	183	L	–	–
152	J	K1	105	168	K	M2	117	184	L	P5	130
153	J	J2	106	169	K	N2	119	185	L	R6	131
154	J	–	–	170	K	–	–	186	L	–	–
155	J	K2	107	171	K	P2	121	187	L	P6	132
156	J	–	–	172	K	–	–	188	L	–	–
157	J	K3	108	173	K	N3	122	189	L	N6	134
158	J	L1	109	174	K	P3	123	190	L	R7	135
159	J	–	–	175	K	–	–	191	L	–	–
160	J	M1	112	176	K	P4	124	192	L	P7	136

Features

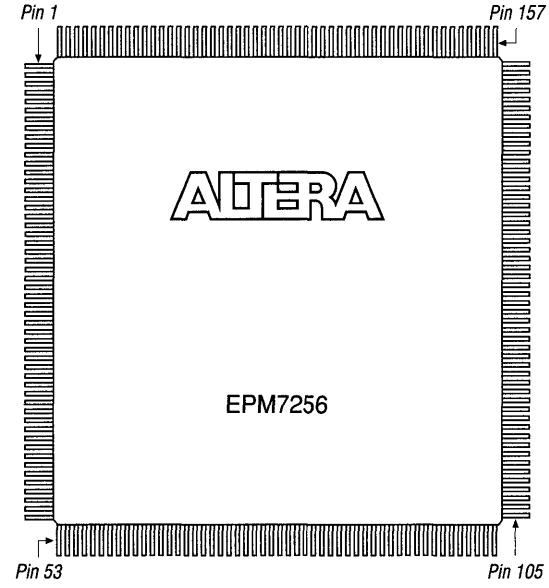
- High-density, erasable CMOS EPLD based on second-generation Multiple Array MatriX (MAX) architecture
  - 5,000 usable gates
  - Combinatorial speeds with t_{PD} = 20 ns
  - Clock frequencies up to 62.5 MHz
- Advanced 0.8-micron CMOS EPROM technology
- Programmable I/O architecture with up to 164 inputs or 160 outputs
- 256 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in 192-pin pin-grid array (PGA) or 208-pin metal quad flat pack (MQFP) packages (see Figure 33)

Figure 33. EPM7256 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 13 and 14 in this data sheet for pin-out information.



192-Pin PGA



208-Pin QFP

General Description

The Altera EPM7256 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 34. Fabricated on a 0.8-micron EPROM technology, the EPM7256 provides 5,000 usable gates, in-system speeds of 62.5 MHz and propagation delays of 20 ns. The EPM7256 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 256 macrocells, the EPM7256 implements complete system-level designs. It

easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to MACH devices and FPGAs. The high density and high I/O pin count make the EPM7256 appropriate for prototyping gate arrays. The EPM7256 can accommodate both logic- and I/O-intensive designs.

Figure 34. EPM7256 Block Diagram

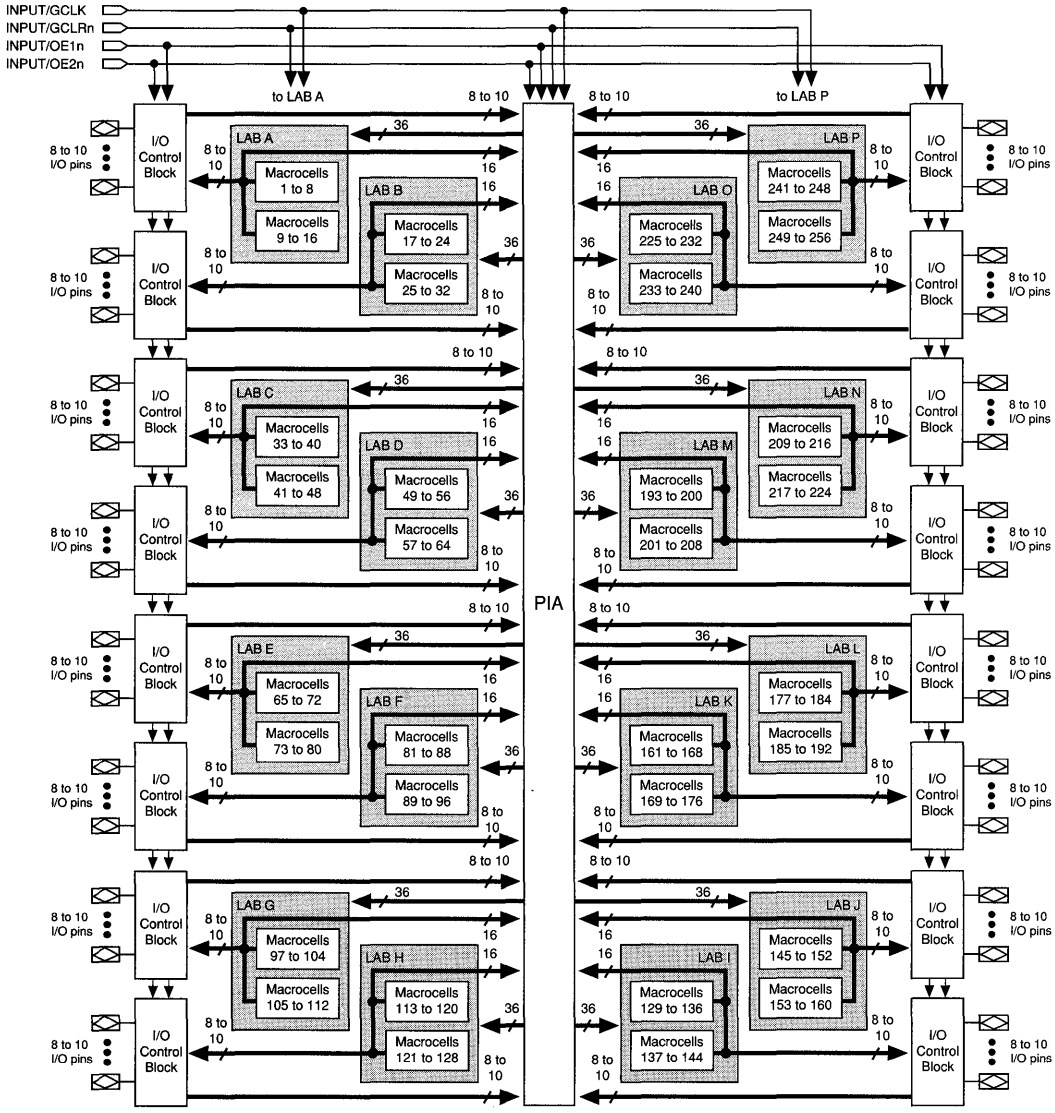


Figure 35 shows the output drive characteristics of EPM7256 I/O pins.

Figure 35. EPM7256 Output Drive Characteristics

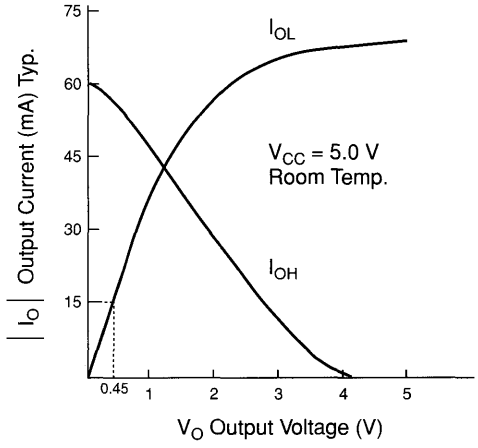


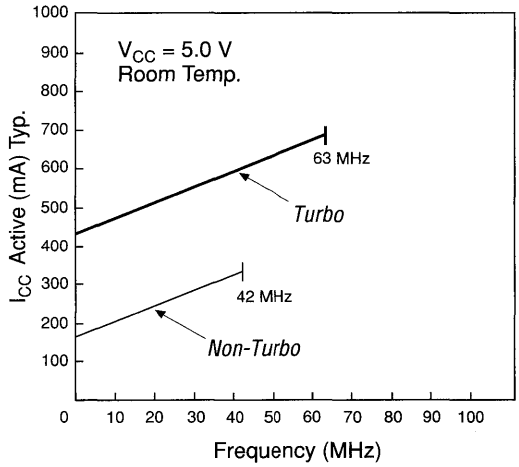
Figure 36 shows typical supply current versus frequency for the EPM7256.

Figure 36. EPM7256 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (1.7 \times MC_{TON}) + (0.59 \times MC_{TOFF}) + [(0.015 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings See *Note (1)* and *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load *Note (5)*		150	225	mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *Note (5)*		155	235	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM7256-2		EPM7256		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	ns
t_{PD2}	I/O input to non-registered output			20		25	ns
t_{SU}	Global clock setup time		12		15		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		12		15	ns
t_{CH}	Global clock high time		6		8		ns
t_{CL}	Global clock low time		6		8		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	ns
t_{ACH}	Array clock high time		8		12.5		ns
t_{ACL}	Array clock low time		8		12.5		ns
t_{CNT}	Minimum global clock period			16		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	62.5		50		MHz
t_{ACNT}	Minimum array clock period			16		25	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	62.5		40		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	83.3		62.5		MHz

Internal Timing Parameters			EPM7256-2		EPM7256		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Shared expander delay			8		10	ns
t_{PEXP}	Parallel expander delay			2		3	ns
t_{LAD}	Logic array delay			8		10	ns
t_{LAC}	Logic control array delay			8		10	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		6	ns
t_{ZX}	Output buffer enable delay			9		12	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		9		12	ns
t_{SU}	Register setup time		4		5		ns
t_{H}	Register hold time		5		6		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{IC}	Array clock delay			8		10	ns
t_{EN}	Register enable time			8		10	ns
t_{GLOB}	Global control delay			3		4	ns
t_{PRE}	Register preset time			4		4	ns
t_{CLR}	Register clear time			4		4	ns
t_{PIA}	Prog. Interconnect Array delay			3		4	ns
t_{LPA}	Low power adder	*Note (8)*		7		8	ns

Notes to tables:

(1) Operation outside the absolute maximum ratings may permanently damage the device. Extended operation at absolute maximum ratings may impair device reliability.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.

(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.

(5) Measured with a device programmed as a 16-bit loadable, enabled, up/down counter in each LAB at 0° C.

(6) Capacitance measured at 25° C. Sample-tested only. The OE1n pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

(7) The f_{MAX} values represent the highest frequency for pipelined data.

(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7256, EPM7256-2
Industrial	(–40° C to 85° C)	EPM7256
Military	(–55° C to 125° C)	Consult factory

Pin-Out Information

Tables 13 and 14 provide pin-out information for the EPM7256 packages.

Table 13. EPM7256 Dedicated Pin-Outs

Dedicated Pin	192-Pin PGA	208-Pin QFP
GCLK	P9	181
GCLRn	R9	183
OE1n	T9	182
OE2n	U9	184
GND	C7, C13, D4, D8, D10, G14, H4, K14, L4, P8, P10, P15, R4, R11	5, 23, 41, 63, 75, 82, 85, 107, 125, 143, 165, 180, 185, 191
VCC	C5, C11, D7, D11, D14, G4, H14, K4, L14, P3, P7, P11, R5, R14	14, 32, 50, 72, 74, 83, 94, 116, 134, 152, 174, 179, 186, 200
No Connect (N.C.)		1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208

Table 14. EPM7256 Pin-Outs (Part 1 of 3)

MC	LAB	192-Pin PGA	208-Pin QFP	MC	LAB	192-Pin PGA	208-Pin QFP	MC	LAB	192-Pin PGA	208-Pin QFP
1	A	U17	4	17	B	N17	16	33	C	B17	49
2	A	–	–	18	B	–	–	34	C	–	–
3	A	R16	3	19	B	M16	15	35	C	C15	48
4	A	–	–	20	B	–	–	36	C	–	–
5	A	P14	206	21	B	M15	13	37	C	C17	47
6	A	U16	205	22	B	P17	12	38	C	C16	46
7	A	–	–	23	B	–	–	39	C	–	–
8	A	R15	204	24	B	N16	11	40	C	D17	45
9	A	U15	203	25	B	R17	10	41	C	D15	44
10	A	–	–	26	B	–	–	42	C	–	–
11	A	T15	202	27	B	P16	9	43	C	E17	43
12	A	–	–	28	B	–	–	44	C	–	–
13	A	U14	201	29	B	T17	8	45	C	D16	42
14	A	U13	199	30	B	N15	7	46	C	E15	40
15	A	–	–	31	B	–	–	47	C	–	–
16	A	T14	198	32	B	T16	6	48	C	F16	39
49	D	A14	65	65	E	U12	197	81	F	J16	27
50	D	–	–	66	E	–	–	82	F	–	–
51	D	B12	64	67	E	R13	196	83	F	J15	26
52	D	–	–	68	E	–	–	84	F	–	–
53	D	B13	62	69	E	U11	195	85	F	K17	25
54	D	A15	61	70	E	T13	194	86	F	J14	24
55	D	–	–	71	E	–	–	87	F	–	–
56	D	B14	60	72	E	T11	193	88	F	K16	22
57	D	A16	59	73	E	T12	192	89	F	K15	21
58	D	–	–	74	E	–	–	90	F	–	–
59	D	C14	58	75	E	R12	190	91	F	L17	20
60	D	–	–	76	E	–	–	92	F	–	–
61	D	B16	57	77	E	U10	189	93	F	L16	19
62	D	B15	56	78	E	R10	188	94	F	M17	18
63	D	–	–	79	E	–	–	95	F	–	–
64	D	A17	55	80	E	T10	187	96	F	L15	17

Table 14. EPM7256 Pin-Outs (Part 2 of 3)

MC	LAB	192-Pin PGA	208-Pin QFP	MC	LAB	192-Pin PGA	208-Pin QFP	MC	LAB	192-Pin PGA	208-Pin QFP
97	G	E16	38	113	H	C9	78	129	I	U6	168
98	G	–	–	114	H	–	–	130	I	–	–
99	G	F17	37	115	H	D9	77	131	I	T5	169
100	G	–	–	116	H	–	–	132	I	–	–
101	G	F15	36	117	H	C10	76	133	I	U7	170
102	G	G16	35	118	H	A10	73	134	I	T6	171
103	G	–	–	119	H	–	–	135	I	–	–
104	G	G15	34	120	H	A11	71	136	I	T7	172
105	G	G17	33	121	H	B10	70	137	I	R6	173
106	G	–	–	122	H	–	–	138	I	–	–
107	G	H17	31	123	H	A12	69	139	I	R7	175
108	G	–	–	124	H	–	–	140	I	–	–
109	G	H15	30	125	H	B11	68	141	I	U8	176
110	G	J17	29	126	H	A13	67	142	I	R8	177
111	G	–	–	127	H	–	–	143	I	–	–
112	G	H16	28	128	H	C12	66	144	I	T8	178
145	J	J2	130	161	K	F3	119	177	L	B9	79
146	J	–	–	162	K	–	–	178	L	–	–
147	J	J3	131	163	K	F1	120	179	L	C8	80
148	J	–	–	164	K	–	–	180	L	–	–
149	J	K1	132	165	K	E2	121	181	L	A9	81
150	J	J4	133	166	K	G2	122	182	L	A8	84
151	J	–	–	167	K	–	–	183	L	–	–
152	J	K2	135	168	K	G3	123	184	L	A7	86
153	J	K3	136	169	K	G1	124	185	L	B8	87
154	J	–	–	170	K	–	–	186	L	–	–
155	J	L1	137	171	K	H1	126	187	L	A6	88
156	J	–	–	172	K	–	–	188	L	–	–
157	J	L2	138	173	K	H3	127	189	L	B7	89
158	J	M1	139	174	K	J1	128	190	L	A5	90
159	J	–	–	175	K	–	–	191	L	–	–
160	J	L3	140	176	K	H2	129	192	L	C6	91

Table 14. EPM7256 Pin-Outs (Part 3 of 3)

MC	LAB	192-Pin PGA	208-Pin QFP	MC	LAB	192-Pin PGA	208-Pin QFP
193	M	U1	153	209	N	N1	141
194	M	–	–	210	N	–	–
195	M	R2	154	211	N	M2	142
196	M	–	–	212	N	–	–
197	M	R3	159	213	N	M3	144
198	M	U2	160	214	N	P1	145
199	M	–	–	215	N	–	–
200	M	P4	161	216	N	N2	146
201	M	U3	162	217	N	R1	147
202	M	–	–	218	N	–	–
203	M	T3	163	219	N	P2	148
204	M	–	–	220	N	–	–
205	M	U4	164	221	N	T1	149
206	M	U5	166	222	N	N3	150
207	M	–	–	223	N	–	–
208	M	T4	167	224	N	T2	151
225	O	B1	108	241	P	A4	92
226	O	–	–	242	P	–	–
227	O	C3	109	243	P	B6	93
228	O	–	–	244	P	–	–
229	O	C1	110	245	P	B5	95
230	O	D3	111	246	P	A3	96
231	O	–	–	247	P	–	–
232	O	D1	112	248	P	B4	97
233	O	C2	113	249	P	A2	98
234	O	–	–	250	P	–	–
235	O	E1	114	251	P	C4	99
236	O	–	–	252	P	–	–
237	O	E3	115	253	P	B2	100
238	O	D2	117	254	P	B3	101
239	O	–	–	255	P	–	–
240	O	F2	118	256	P	A1	102

Notes:

EPM7032V EPLD

3.3-Volt 32-Macrocell Device

February 1993, ver. 2 Data Sheet

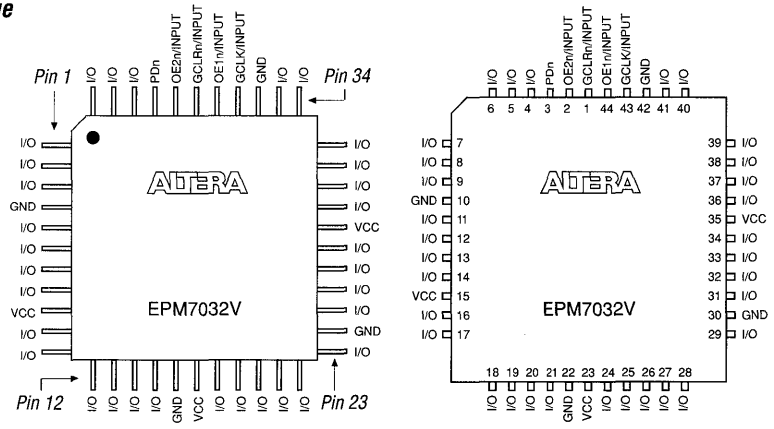
Features...

Preliminary Information

- 3.3-V version of the popular EPM7032 EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Clock frequencies up to 71 MHz
- Innovative power-saving features
  - 30% to 50% power savings over 5-V operation
  - Power-down mode controlled by a power-down pin to allow zero power consumption during periods of inactivity
  - Programmable power-saver mode for 50% or more power reduction during active operation, configurable for each macrocell
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture allowing up to 36 inputs or 32 outputs
- 32 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Programmable registers configurable as D, T, JK, and SR flipflops with individual Clear, Preset, Clock, and Clock Enable controls
- Independent clocking of all registers from array or global Clock signals
- Available in 44-pin plastic EIAJ-standard thin quad flat pack (TQFP) and plastic J-lead chip carrier (PLCC) reprogrammable packages (see Figure 1)
- Pin-, function-, and POF-compatible with 5-V EPM7032 device. A 44-pin thin quad flat pack (TQFP) is under development.

Figure 1. EPM7032V Package Pin-Out Diagrams

Package outlines not drawn to scale.



...and More Features

- Software design support featuring Altera's MAX+PLUS II development system on PC, Sun SPARCstation, and HP 9000 Series 700 platforms
- Programming support from Altera's Master Programming Unit (MPU) or programming hardware from other manufacturers

General Description

The EPM7032V is a high-performance MAX 7000 EPLD that meets the low power and voltage requirements of 3.3-V applications ranging from notebook computers to battery-operated, hand-held equipment. Fabricated on a 0.8-micron EEPROM technology, the EPM7032V provides in-system speeds up to 71 MHz and propagation delays of 15 ns. Its architecture supports 100% TTL emulation and can integrate SSI, MSI, and custom logic functions. The EPM7032V can replace multiple 20- and 24-pin PLDs. It is available in 44-pin reprogrammable PLCC or TQFP packages and can accommodate designs with up to 36 inputs and 32 outputs.

The EPM7032V uses CMOS EEPROM cells to implement logic functions within the device. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The EPM7032V can be reprogrammed for quick and efficient iterations during design development and debug cycles. Each device is guaranteed for 100 program and erase cycles.

The EPM7032V consists of 32 macrocells grouped into two Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides D, T, JK, or SR operation with independent programmable Clock, Clock Enable, Clear, and Preset functions. To build complex logic functions, each macrocell can be supplemented with both shared and high-speed parallel expander product terms that provide up to 32 product terms per macrocell.

The EPM7032V provides a unique power-down mode that is ideal for power-sensitive applications. Externally controlled by a dedicated power-down pin (PDn), the device can be powered down to a near-zero-power consumption level, typically 50 µA. While in power-down mode, all internal logic and external I/O signals of the EPM7032V maintain the state just prior to the assertion of the power-down pin. When this pin is released, the device resumes normal operation.

The EPM7032V also provides programmable speed and power optimization. Speed-critical portions of a design can run at high speed and full power, while the remainder runs at reduced speed and low power. This feature enables the user to configure individual macrocells to operate at 50% or less power while adding only a nominal timing delay.

The EPM7032V is supported by Altera's MAX+PLUS II development system, which offers schematic, text, and waveform design entry; compilation and logic synthesis; simulation; and programming software, all in a single integrated package. MAX+PLUS II provides an EDIF, VHDL,

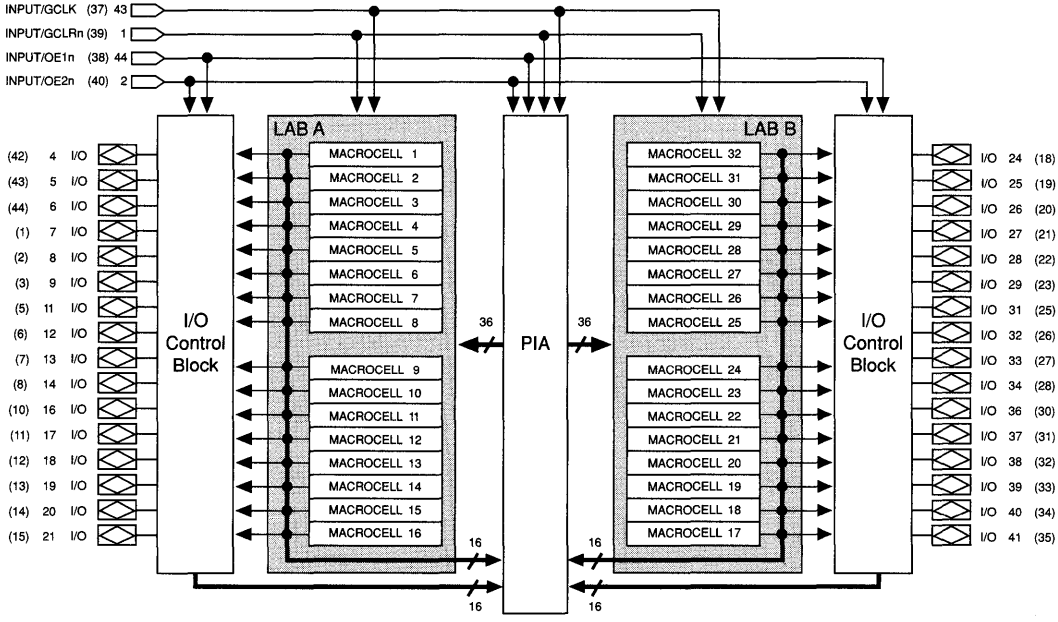
and Verilog netlist interface for additional design entry and simulation support from other industry-standard PC- and workstation-based CAE tools. The system runs on 386- and 486-based PCs or Sun SPARCstations and HP 9000 Series 700 workstations.

Functional Description

The EPM7032V is a 32-macrocell EPLD that is optimized for integrating multiple TTL, PAL, and GAL devices (see Figure 2). It has 32 I/O pins that can be individually configured for input, output, or bidirectional operation. The EPM7032V also has 4 dedicated input pins that can be programmed as general-purpose inputs or high-speed global control signals (Clock, Clear, and 2 Output Enable signals) for each macrocell and I/O pin.

Figure 2. EPM7032V Block Diagram

Pin numbers are for the J-lead package. Pin numbers in parentheses are for the QFP package.



The EPM7032V architecture includes the following elements:

- Logic Array Blocks
- Macrocells
- Expander product terms (shared and parallel)
- Programmable Interconnect Array
- I/O control blocks

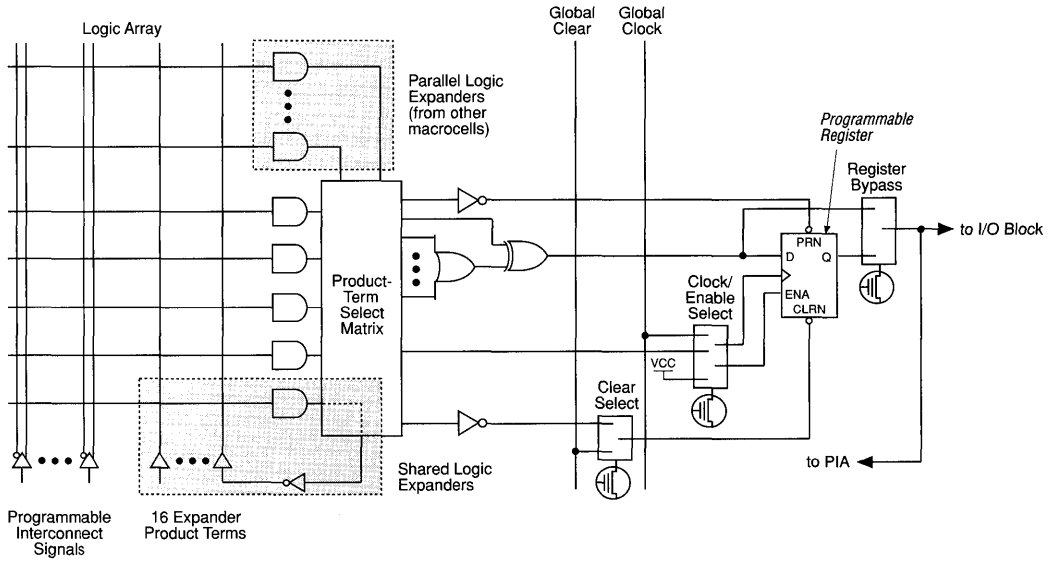
Logic Array Blocks

MAX 7000 architecture is based on the concept of linking high-performance, flexible logic array modules called Logic Array Blocks (LABs). Multiple LABs are linked together via the Programmable Interconnect Array (PIA), a global bus that is fed by all EPM7032V dedicated inputs, I/O pins, and macrocells. All inputs to each LAB, except the global control signals, are fed by 36 signals from the PIA.

Macrocells

The MAX 7000 macrocell, shown in Figure 3, can be individually configured for both sequential and combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Figure 3. MAX 7000 Macrocell



Combinatorial logic is implemented in the logic array, which contains five product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs for the macrocell's register Clear, Preset, Clock, and Clock Enable control functions. One product term per macrocell can be inverted and fed directly back into the logic array. These "shared expander" product terms can be connected

to any other product term within the LAB. Based on the logic requirements of the design, MAX+PLUS II automatically optimizes product-term allocation.

In registered functions, each macrocell flipflop can be individually programmed for D, T, JK, or SR operation with programmable Clock control. If necessary, the flipflop can be bypassed for combinatorial operation. During design entry, the user can specify the desired flipflop type or allow MAX+PLUS II to select the most efficient flipflop operation for each registered logic function to minimize the resources needed by the design.

Three clocking modes are available for each programmable register:

- A register can be clocked by the dedicated global Clock pin (GCLK). In this mode, the flipflop is positive-edge-triggered, and offers the fastest Clock-to-output performance.
- A register can be clocked by an array Clock implemented with a product term. In this mode, the flipflop can be configured for positive- or negative-edge-triggered operation. Array Clocks allow any signal source within the device or gated logic functions to clock the flipflop.
- A register can be clocked by a global Clock pin and enabled by a product term. The register is enabled when the flipflop's Clock Enable (ENA) input is high. Each flipflop can be activated individually while taking advantage of the fast Clock-to-output delay of the global Clock pin.

Each register also supports asynchronous Preset and Clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the register is designed for active-low Preset and Clear, active-high control is also provided when the signal is inverted within the logic array. In addition, each register Clear function can be individually driven by the active-low dedicated global Clear pin (GCLRn).

Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Instead of using another macrocell to supply the needed logic resources, the MAX 7000 architecture offers both shared and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has up to 16 shareable expanders, which can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverting outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shareable expanders can also be cross-coupled to build additional buried flipflops, latches, or input registers. A small delay (t_{SEXP}) is incurred when shareable expanders are used.

Parallel Expanders

Parallel logic expanders are unused product terms from macrocells in the LAB, which the product-term select matrix can allocate to any macrocell to implement fast, complex logic functions. With parallel expanders, up to 20 product terms can directly feed the macrocell OR logic—5 product terms from the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can automatically route parallel expanders to the necessary macrocells in sets of 1 to 5. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms, the second set 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within the LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel logic expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, macrocells 7 and 6, or macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders; the highest-numbered macrocells can only borrow them.

Programmable Interconnect Array

Logic is routed between LABs on the Programmable Interconnect Array (PIA). This global bus is a programmable path that routes any signal source to any destination on the device. All EPM7032V dedicated inputs, I/O pin feedbacks, and macrocell feedbacks feed the PIA and are routed across the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB.

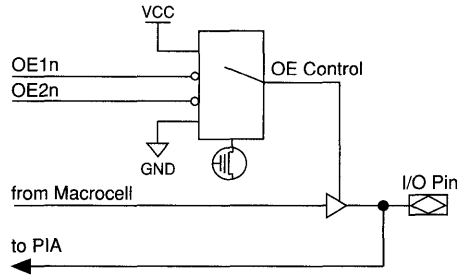
While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the EPM7032V PIA has a fixed delay. The PIA thus

eliminates skew between signals, and makes timing performance easy to predict.

I/O Control Blocks

The I/O control block, shown in Figure 4, allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is connected to one of two global active-low Output Enable pins (OE1n and OE2n) or directly to GND or VCC. When the tri-state buffer is connected to GND, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer is connected to VCC, the output is enabled.

Figure 4. I/O Control Block



The EPM7032V provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Power Management

The 3.3-V operation of the EPM7032V offers power savings of 30% to 50% over the 5-V operation of the EPM7032. Additional power-saving features of the EPM7032V include a programmable power-saver mode and a power-down mode.

Power-Saver Mode

The EPM7032V offers a power-saver mode that supports low-power operation across user-defined signal paths or the entire device. This feature can reduce total power dissipation by 50% or more, since most logic applications require only a fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in the EPM7032V for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while

remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters.

Power-Down Mode

The EPM7032V provides a power-down mode that allows the device to consume near-zero power (typically 50 µA). The power-down mode is controlled externally by the dedicated power-down pin (PDn). When PDn is asserted (i.e., brought to ground), the power-down sequence latches all inputs, internal logic, and output pins of the EPM7032V, preserving their present state. Output pins maintain their present low, high, or tri-state (high-impedance) value while in power-down mode. Once in power-down mode, any or all of the inputs, including Clocks, can be toggled without affecting the frozen state of the device. Since internal latches are used to ensure that the proper state exists during power-down mode, the external inputs and Clocks must meet certain setup and hold time requirements. For more information, refer to the timing diagram in Figure 6, the Power-Down Timing Parameters table, and the Chip Enable Timing Parameters table, which appear later in this data sheet.

When the device is enabled, the PDn signal is brought high, and the combinatorial outputs respond to the present input conditions within the specified chip enable delay (t_{CE}). Registered outputs respond to Clock transitions within t_{CE}. Clocking the device during the chip enable sequence can cause the data to change internal to the chip if a Clock transition occurs during certain intervals of the chip enable or chip disable sequences. All Clocks should be gated to prevent Clock transitions during the Clock setup time (t_{GCSUPD} or t_{ACSUPD}) and t_{CE} after the chip enable setup time (t_{GCSTCE} or t_{ACSTCE}). These periods are shown in Figure 6. All registers in the EPM7032V provide Clock Enable control for simple access to disable Clocks. If output signals must be frozen in a high-impedance state during power-down, the associated Output Enable signal must be asserted, the system Clock removed, and then the PDn pin asserted. To reactivate the device, the sequence is reversed. For some systems, it may be more appropriate to switch the order of the Clock and Output Enable controls.

All power-down/chip enable timing parameters are computed from external inputs or I/O pins, with the macrocell Turbo Bit turned on, and without the use of parallel expanders. For macrocells in low-power mode (Turbo Bit off), the low-power adder t_{LPA} must be added to power-down/chip enable timing parameters, which include the data paths t_{LAD}, t_{LAC}, t_{ACL}, t_{ACH}, and t_{SEXP}. For macrocells using parallel expanders, t_{PEXP} must be added. For data or Clock paths using more than one logic array delay, the worst-case data or Clock delay also must be added to the respective power-down/chip enable parameters. Actual worst-case timing for data

and Clock paths can be calculated with the MAX+PLUS II Timing Simulator or Timing Analyzer, or other industry-standard CAE verification tools.

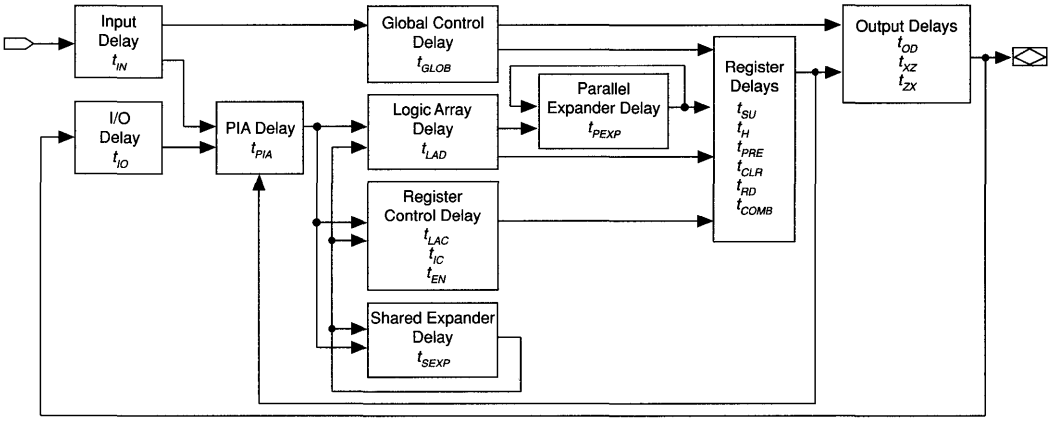
Design Security

The EPM7032V contains a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EEPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when the device is erased.

Timing Model

EPM7032V timing can be analyzed with MAX+PLUS II software, with a variety of popular industry-standard CAE simulators and timing analyzers, or with the timing model shown in Figure 5. The EPM7032V has fixed internal delays that allow the user to determine the worst-case timing for any design. For complete timing information, MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 5. MAX 7000 Timing Model



Timing information can be calculated with the timing model and the timing parameters for a particular device. External timing parameters are derived from the sum of internal parameters and represent pin-to-pin timing delays. Figure 6 shows the internal timing relationship for internal and external delay parameters. Actual worst-case timing can be calculated in a timing simulation with the MAX+PLUS II Simulator, in a timing analysis with the MAX+PLUS II Timing Analyzer, or with other industry-standard CAE tools.

Figure 6. Switching Waveforms (Part 1 of 2)

t_R & t_F < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

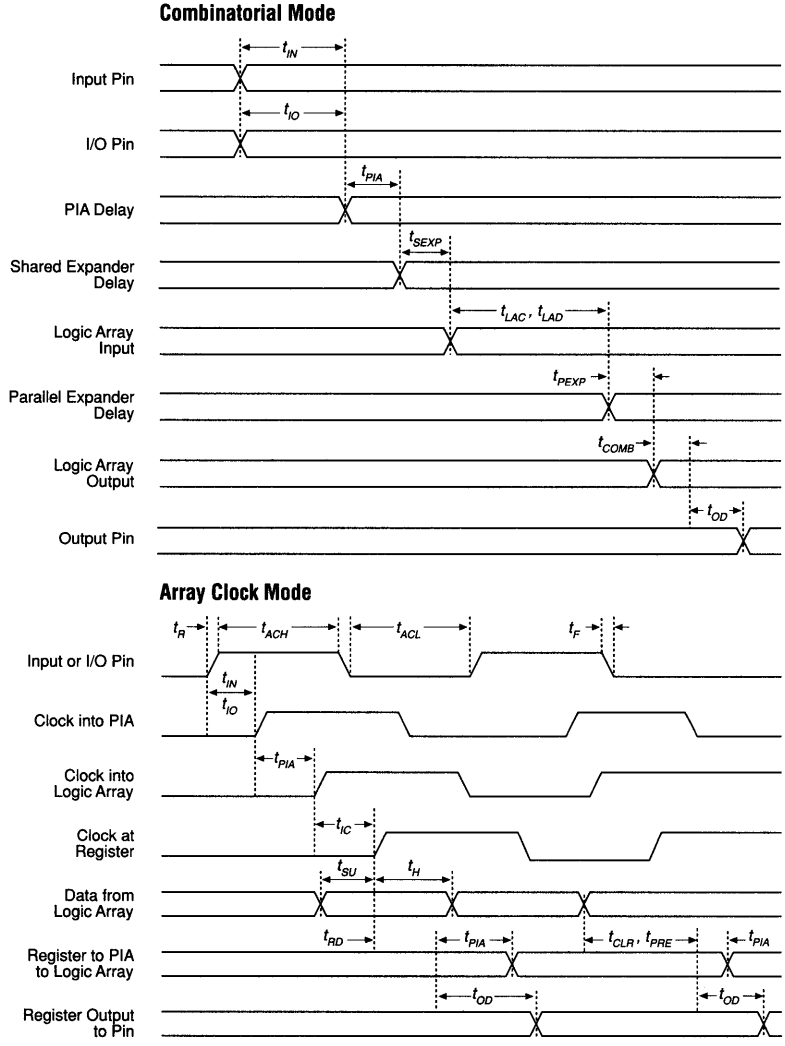
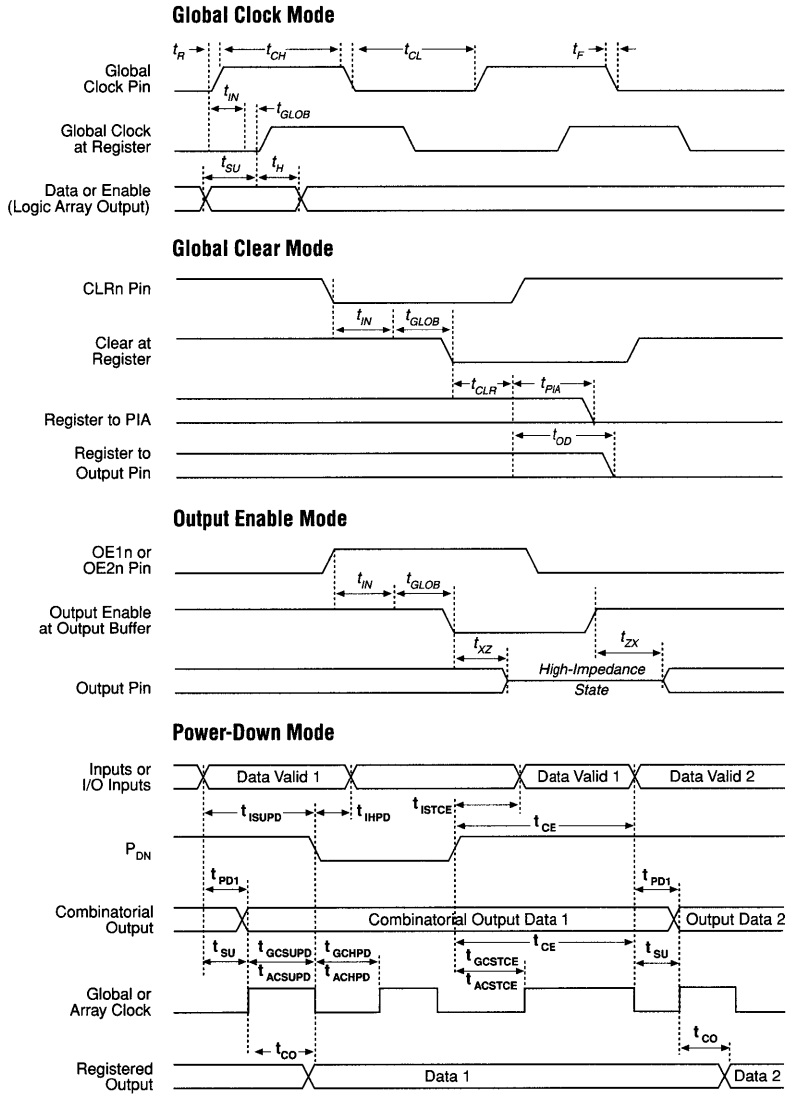


Figure 6. Switching Waveforms (Part 2 of 2)



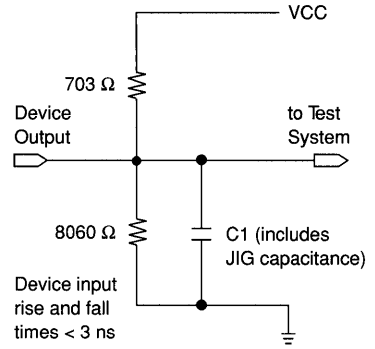
Generic Testing

The EPM7032V is functionally tested and guaranteed. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under the conditions shown in Figure 7.

Test patterns can be used and then erased during the early stages of the production flow. This facility to use application-independent, general-purpose tests, called generic testing, is unique among user-configurable logic devices.

Figure 7. EPM7032V AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



MAX+PLUS II Development System

The EPM7032V device is supported by Altera's MAX+PLUS II development system, which offers schematic, text, and waveform design entry; compilation and logic synthesis; simulation; and programming software in a single integrated package. MAX+PLUS II also provides an EDIF netlist interface for additional design entry and simulation support by other industry-standard CAE tools from vendors such as Cadence, Data I/O, Intergraph, Exemplar, Mentor Graphics, OrCAD, Synopsys, and Viewlogic. In addition, MAX+PLUS II also exports Verilog or VHDL netlist files to support simulation with the Cadence Verilog-XL simulator or various VHDL simulators. The system runs on 386- and 486-based PCs or Sun SPARCstations and HP 9000 Series 700 workstations. For further details about MAX+PLUS II, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Device Programming

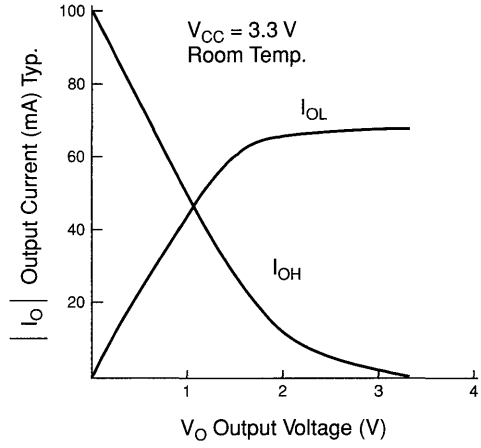
EPM7032V devices can be programmed on 386- or 486-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU supports open- and short-circuit testing, and performs continuity checking to ensure adequate electrical contact between the adapter and the device.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 EPLD with the results of simulation.

Data I/O and other programming hardware manufacturers also provide programming support for Altera devices. See *Programming Hardware Manufacturers* in this data book for more information.

Figure 8 shows the output drive characteristics of EPM7032V I/O pins.

Figure 8. Typical EPM7032V Output Drive Characteristics



Absolute Maximum Ratings

See *Note (1)* and *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions

Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –0.1 mA DC	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC0}	V_{CC} supply current (standby, power-down mode)			50		µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load, *Note (5)*		10		mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *Note (5)*		15		mA

Capacitance

Note (6)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM7032V-3		EPM7032V-4		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	ns
t_{PD2}	I/O input to non-registered output			15		20	ns
t_{SU}	Global clock setup time		11		12		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8		12	ns
t_{CH}	Global clock high time		5		6		ns
t_{CL}	Global clock low time		5		6		ns
t_{ASU}	Array clock setup time		4		5		ns
t_{AH}	Array clock hold time		4		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		20	ns
t_{ACH}	Array clock high time		6		8		ns
t_{ACL}	Array clock low time		6		8		ns
t_{CNT}	Minimum global clock period			13		16	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			13		16	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	100		83.3		MHz

Internal Timing Parameters			EPM7032V-3		EPM7032V-4		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		3	ns
t_{IO}	I/O input pad and buffer delay			2		3	ns
t_{SEXP}	Shared expander delay			8		9	ns
t_{PEXP}	Parallel expander delay			1		2	ns
t_{LAD}	Logic array delay			6		8	ns
t_{LAC}	Logic control array delay			6		8	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		5	ns
t_{ZX}	Output buffer enable delay			6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		9	ns
t_{SU}	Register setup time		4		4		ns
t_{H}	Register hold time		4		5		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{IC}	Array clock delay			6		8	ns
t_{EN}	Register enable time			6		8	ns
t_{GLOB}	Global control delay			1		3	ns
t_{PRE}	Register preset time			4		4	ns
t_{CLR}	Register clear time			4		4	ns
t_{PIA}	Prog. Interconnect Array delay			2		3	ns
t_{LPA}	Low power adder	*Note (8)*		9		11	ns

Power-Down/Chip Enable Timing Parameters

Power-Down Timing Parameters		EPM7032V-3		EPM7032V-4		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{ISUPD}	Input or I/O input setup time before power down	30		35		ns
t_{IHPD}	Input or I/O input hold time after power down	0		0		ns
t_{GCSUPD}	Global clock setup time before power down	20		25		ns
t_{GCHPD}	Global clock hold time after power down	0		0		ns
t_{ACSUPD}	Array clock setup time before power down	30		35		ns
t_{ACHPD}	Array clock hold time after power down	0		0		ns
t_{HPD}	Minimum high pulse width of power-down pin	800		900		ns
t_{LPD}	Minimum low pulse width of power-down pin	800		900		ns
t_{PDOWN}	Power down delay		800		900	ns

Chip Enable Timing Parameters		EPM7032V-3		EPM7032V-4		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{ISTCE}	Input or I/O input stable after chip enable		60		70	ns
t_{GCSTCE}	Global clock stable after chip enable		60		70	ns
t_{ACSTCE}	Array clock stable after chip enable		60		70	ns
t_{CE}	Data stable after chip enable		700		800	ns

Notes to tables:

(1) Operation outside the absolute maximum ratings may permanently damage the device. Extended operation at absolute maximum ratings may impair device reliability.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) Typical values are for $T_A = 25°$ C and $V_{CC} = 3.3$ V.

(4) Operating conditions: $V_{CC} = 3.3$ V ± 10%, $T_A = 0°$ C to 70° C for commercial use.
$V_{CC} = 3.3$ V ± 10%, $T_A = -40°$ C to 85° C for industrial use.

(5) Measured with a device programmed as a 16-bit loadable, enabled, up/down counter in each LAB.

(6) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

(7) The f_{MAX} values represent the highest frequency for pipelined data.

(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7032V-3, EPM7032V-4
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Operating Requirements for Altera Devices

February 1993 Data Sheet

Introduction

Altera devices combine unique programmable logic architectures with advanced CMOS processes to provide exceptional performance and reliability. To maintain the highest possible performance and reliability of Altera devices, system designers must consider the following operating requirements:

- Operating conditions
- Voltage levels on pins
- Output loading
- Power supply management
- Thermal analysis and prevention of heat build-up
- Device erasure

Operating Conditions

Altera devices are rated according to a set of defined parameters, which must be considered when a device is implemented in a system. These parameters are provided in each device data sheet and include absolute maximum ratings, recommended operating conditions, and DC and AC operating conditions.

Absolute Maximum Ratings

Absolute maximum ratings define the limits of the conditions that a particular Altera device can withstand. These values are based on experimental evidence of device behavior, as well as theoretical modeling of breakdown and damage mechanisms. These ratings are stress ratings only. Functional operation of the device at these conditions or at conditions above those indicated in the "Recommended Operating Conditions" table in the individual device data sheet is not implied. For example, I_{OUT} is the absolute current capacity and is not the drive capability of an output pin. The output source and sink currents are given as I_{OH} and I_{OL} in the "DC Operating Conditions" section of each data sheet.

Operating an Altera device at conditions listed in the "Absolute Maximum Ratings" table for extended periods of time may impair device reliability. Operating the device at conditions that exceed these ratings may cause permanent damage to the device.

Recommended Operating Conditions

The functional operation limits for an Altera device, given in the "Recommended Operating Conditions" table in the individual device data sheet, specify limits under which all AC and DC parameters are guaranteed. These parameters may also be expressed differently in other rating sections. For example, the V_{CC} range specified in this table is the range over which the AC and DC Operating Conditions are guaranteed. The V_{CC} range specified in the "Absolute Maximum Ratings" table is the power supply level beyond which the device will be damaged.

DC Operating Conditions

The steady-state voltage and current values expected from an Altera device are provided in the "DC Operating Conditions" table in the individual device data sheet. This information includes input voltage sensitivities (V_{IH}, V_{IL}), output voltage (V_{OH}, V_{OL}) and current capability (I_{OH}, I_{OL}), and input and output leakage currents (I_I, I_{OZ}). The values are guaranteed for DC operation under the conditions specified in each device data sheet.

This table also provides standby and active V_{CC} supply current ratings (I_{CC}) for a device that is 100% filled with 16-bit counters. These I_{CC} measurements are taken at the input frequency specified in the device data sheet with all of the outputs disabled.

The values in this section are used during a current-loading analysis, which the designer must perform to estimate the total device current dissipation (see "Power Supply Management" later in this data sheet).

AC Operating Conditions

The external and internal timing parameters for an Altera device are given in the "AC Operating Conditions" tables in the individual device data sheet. These parameters are determined under the conditions specified in the "Recommended Operating Conditions" table and a particular V_{CC} and temperature range. The external timing parameters are guaranteed pin-to-pin delays when the device is operating under these conditions.

Timing parameters are specified as either maximum or minimum values. A maximum value indicates that the delay will not exceed the specified time. A parameter with a maximum value does not have a corresponding minimum value because no lower performance limit exists. Setup, hold, and pulse width times are expressed as minimum values that the system must provide to ensure reliable device operation. These parameters do not have corresponding upper performance limits.

Voltage Levels on Pins

Device pins can be exposed to dangerous voltages during handling or device operation. During handling, pins can be exposed to high-voltage static discharges that cause electrostatic discharge (ESD) damage. During operation, power-supply spikes on the VCC and GND pins or errant logic levels elsewhere in the system can produce logic level stress with voltages on the order of magnitude of V_{CC} (0 to 15 V). To minimize these hazards, the user must observe the precautions specified for the following conditions:

- Pin connections
- Latch-up
- Hot-socketing
- Electrostatic discharge
- Maximum V_{CC} rise time and power-on reset time

Pin Connections

For proper operation, signals on the input and output pins must be in the following range:

$GND < (V_{IN}$ *or* $V_{OUT}) < V_{CC}$

During project compilation, MAX+PLUS II software generates a device utilization report, called a Report File (**.rpt**), that provides information on the pin-outs and connectivity of the device(s) used in the project. The Report File includes a pin-out diagram that shows the signals assigned to each pin, pins that must be tied to V_{CC} or GND, and reserved pins that are left unconnected for possible future use. User pins are identified by the name assigned during design entry. All named pins must be wired as shown in the pin-out diagram to implement the logic correctly in the programmed device.

The VCC and GND pins should be tied to the V_{CC} or GND planes on the printed circuit board (PCB). Dedicated input pins used in a design and I/O pins configured as inputs should always be driven by an active source. I/O pins configured as bidirectional pins should always be driven whenever the I/O pin is acting as an input.

Unused input and I/O pins are marked in the Report File as GND and RESERVED, respectively. Unused inputs should be tied to the GND plane. Otherwise, these pins "float" in an indeterminate state, possibly increasing DC current in the device and introducing noise into the system. Reserved I/O pins should remain unconnected, since they are driven by active signals representing the buried logic present in the logic cell associated with that particular pin. Tying a reserved I/O pin to either V_{CC} or GND creates contention that may damage the output driver on the device.

Latch-Up

Parasitic bipolar transistors, present in the fundamental structure of CMOS devices, may be paths for dangerous currents in the device. Typically, the base-emitter and base-collector junctions of these transistors are not forward-biased, so the transistors are not turned on. Figure 1 shows a cross-section of a CMOS wafer and primary parasitic transistors. To ensure that all junctions remain reverse-biased, the P-type substrate is connected to the most negative voltage available on-chip (GND), and the N-type well structure is connected to the most positive voltage on-chip (V_{CC}).

Figure 1. Parasitic Bipolar Transistors in CMOS

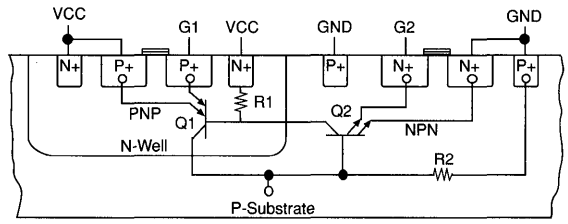


Figure 1 also shows the parasitic resistors that occur in the CMOS structure. Generally, these resistors are of no concern as long as currents do not flow through the structure laterally. However, I-R drops may occur in the structure if any of the associated diodes turn on. These diodes may be initially turned on by power-supply or I/O pin transients that exceed the limits of GND and V_{CC}. These transients can be induced by signal ringing and other inductive effects in the system.

Catastrophic failure can occur if these parasitic structures begin to conduct, since the effect is regenerative and reinforces itself until potentially destructive currents flow. This silicon-controlled rectifier (SCR) effect is called "latch-up." As the current flows through the parasitic transistor, the I-R drop through the resistor increases, further forward-biasing the base-emitter junction. The cycle continues until the current is limited by drops in the primary current path. However, this current may have reached a level that permanently damages internal circuitry.

Altera devices have been designed to minimize the effects of latch-up, including power supply and I/O pin transients. Under recommended operating conditions, all devices are guaranteed to withstand input voltage extremes of between GND – 1 V and V_{CC} + 1 V, as well as input currents of 100 mA or less that are forced through the device pins.

☞ To minimize inducing latch-up during power and input sequencing to the device, apply voltages and logic inputs first to GND, then V_{CC}, and finally to the inputs. Remove power from the device in the reverse order: first, inputs are removed, then V_{CC}, and finally GND.

Simultaneous application of inputs and V_{CC} to the device, which may occur as a power supply rises during power up, should be safe as long as V_{CC} meets the maximum rise time. The user should ensure that inputs cannot rise faster than the supply at the V_{CC} pin(s).

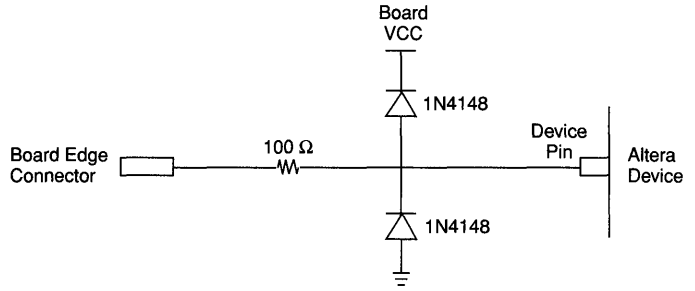
Hot-Socketing

Latch-up frequently occurs when electrical subsystems are plugged into active hardware or "hot-socketed." When a subsystem is plugged into active hardware, the logic levels often appear at the subsystem's logic devices before the power supply can provide current to the V_{CC} and GND grid of the subsystem board. As V_{CC} rises towards the input logic level, the CMOS input structures begin to conduct large amounts of current, producing potentially destructive latch-up.

The chances of latch-up occurring during hot-socketing can be reduced by increasing the length of the V_{CC} and GND connections. If metal "fingers" are used for the board connection, the V_{CC} and GND fingers at the card edge should be longer than the logic connections. This difference in length causes the power supply to appear before the logic levels at a device, and is usually sufficient to prevent latch-up. Off-the-shelf connectors with longer V_{CC} and GND connections can also provide similar results.

Implementing the circuitry shown in Figure 2 also provides protection against latch-up during hot-socketing. The diode structure provides a "clamp" level on the input voltage, preventing it from swinging more than one diode-drop away from a power-rail (–0.6 V to V_{CC} + 0.6 V). The series resistor also reduces the possibility of latch-up by restricting the current to the device input and clamp diodes. This circuitry provides the maximum protection against latch-up, but is usually required only if the input on the device is tied directly to the edge connector. Device inputs that are driven by other circuit elements in the subsystem are generally safe from latch-up, since these elements provide a natural delay before the logic levels are established.

Figure 2. Hot-Socket Protection



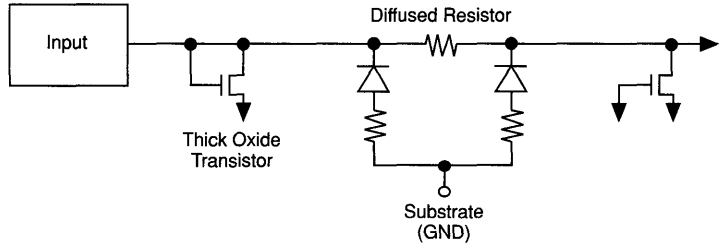
Electrostatic Discharge

Electrostatic discharge (ESD) resulting from improper device handling can cause device failure that may not manifest itself for a long period of time. Although ESD damage may result in immediate device failure, it more frequently affects the long-term reliability of the device.

Device handling during the programming cycle increases exposure to potential static-induced failure. During normal activity, the human body can generate voltages of up to tens of kilovolts (kV). Wearing ground straps during device handling and grounding all surfaces that come in contact with components reduces the likelihood of damage. Synthetic materials used in clothing can store large amounts of static electricity and may also cause ESD.

Altera devices include special structures that reduce the effects of ESD at the pins. Figure 3 shows a typical input structure for an Altera device. Diode structures and specialized field effect transistors shunt harmful voltages to ground before destructive currents can flow. Most Altera devices can withstand ESD voltages greater than 2 kV, but all devices are guaranteed to withstand ESD voltages greater than 1 kV.

Figure 3. Altera Device Input Protection Structure



Maximum V_{CC} Rise Time & Power-On Reset Time

When power is applied to an Altera device, the device initiates a Power-On Reset (POR), typically as V_{CC} approaches 1.5 V to 2.0 V. The POR event is dependent on V_{CC} reaching the recommended operating range (4.75 V to 5.25 V) within a certain period of time (specified as a maximum V_{CC} rise time). Slower rise times can cause incorrect device initialization and functional failure.

☞ The maximum V_{CC} rise time for MAX 7000 devices is 10 ms.

The POR time is the time required after V_{CC} reaches the recommended operating range to clear device registers, configure I/O pins, and release tri-states. Once this initialization is complete, the device is ready to begin logic operation. The POR time is typically no more than 50 ms.

Output Loading

Both resistive and capacitive loading may occur in any electrical circuit. During development, the designer should ensure that the target device can supply both the current and speed necessary for the loads.

Resistive Loading

Resistive loads exist for devices that interface with TTL devices or drive terminated buses and discrete bipolar transistors. Characterized by dissipating DC current, a resistive load dampens the output waveforms, reducing the effects of transients or noise on the signal. Resistive loading reduces the noise on the signal, but the signal is diminished by this process.

Output current capabilities (I_{OH} and I_{OL}), which are functions of output voltages (V_{OH} and V_{OL}), are given in the data sheet for each device. In a DC condition, output current capabilities determine the maximum resistivity of a load while still maintaining the necessary output voltage. If the system requires higher currents, such as those necessary to drive an LED or a relay, a high-current buffer or a discrete current switch must be used.

Short-circuit conditions (where R = 0) can damage the device permanently by drawing too much current through the output buffer. Therefore, short-circuit conditions must be avoided.

Capacitive Loading

The "AC Operating Conditions" table in a device data sheet documents test conditions such as V_{CC} and operating temperature for a particular parameter. An output capacitance condition (C1) is also provided for parameters relating to external performance and I/O pins on the device. For most Altera devices, C1 is 35 pF for active signals and 5 pF for high-impedance parameters.

Package characteristics and trace capacitance contribute the majority of loading capacitance. A small percentage of the total capacitance on output buffers is attributable to the gate capacitance of CMOS device inputs. The specified 35-pF load condition is a representative value for most CMOS circuits. For applications in which an Altera device drives a higher capacitance, performance decreases as the capacitive load increases.

Device sockets are a source of both capacitive and inductive loading. Once a system is finalized for production, sockets should be removed if possible and the devices should be mounted directly onto the PCB. Direct board mounting reduces both the capacitive load and the noise from socket contacts.

To ensure the highest circuit performance, the capacitance on device outputs should be minimized. Since wiring traces on the PCB, device input pins, and device packaging all contribute to the total capacitance, these following guidelines should be observed:

- Board layout should ensure that signals run perpendicular to each other to provide a minimum capacitive coupling effect. Also, signal traces should be kept as short as possible, and V_{CC} and GND planes should be provided (see "Power Supply Management" later in this data sheet for details on V_{CC} and GND planes).

- A high-current buffer should be used to speed the signal to all destinations for networks in which a single source drives many loads.

The lack of V_{CC} and GND planes or excessive trace lengths may cause problems with radiated coupling of noise into logic signals and transmission-line effects on signal quality. These ringing and noise elements on logic levels can lead to circuit reliability problems. When recommended layout practices cannot be implemented to prevent transmission-line problems, a small series resistance (10 to 30 Ω) can be used to reduce the magnitude of undershoot and overshoot on signal edges. This resistance dampens the ringing that can occur on long board traces and prevents false triggering.

Power Supply Management

Although Altera devices are designed to minimize noise generation and susceptibility, they—like all CMOS devices—can be sensitive to fluctuations in power supply and input lines. To minimize the effect of these fluctuations, the system designer must pay special attention to:

- V_{CC} and GND planes
- Decoupling capacitors
- Current dissipation

V_{CC} & GND Planes

The system designer can minimize power supply noise or "ground bounce" by providing separate V_{CC} and GND planes for every PCB, thus ensuring a near-infinite current sink capability, noise protection, and shielding for logic signals on the board. If an entire plane cannot be provided, the widest possible GND and V_{CC} traces should be created throughout the entire board. Logic-width traces should not be used to carry the power supply. Although V_{CC} and GND planes tend to increase the capacitive load of the traces, they significantly reduce system noise, and dramatically increase system reliability.

Decoupling Capacitors

Each VCC and GND pin should be connected directly to the V_{CC} and GND planes in the PCB. Each pair of VCC and GND pins should be decoupled with a 0.2-µF power-supply decoupling capacitor, located as close as possible to the Altera device. For effective decoupling of the power supply, one capacitor per VCC and GND pair must be provided. Decoupling capacitors with a good frequency response, such as those found in monolithic-ceramic capacitors, should be used.

Every PCB should also have a large-capacity, general-purpose, electrolytic capacitor network to stabilize the power supply. A 100-µF capacitor can be placed immediately adjacent to the location where the power supply lines come into the PCB. If a transformer or regulator is used to change the voltage level, the capacitor should be placed immediately after the final stage that develops the device's V_{CC} supply. A large electrolytic capacitor serves as a restoring force in the power grid. It pulls up a sagging power supply by providing current when necessary, and pulls back a peaking supply by storing the excess current. This capacitor provides a beneficial leveling effect that supplies extra current whenever a large number of nodes start switching in a circuit. However, the larger the power supply capacitor, the longer it takes to bring the maximum V_{CC} to the operating level. The capacitor should not violate the V_{CC} rise time discussed in "Voltage Levels on Pins" earlier in this data sheet.

Current Dissipation

Every Altera device is designed to consume the least possible amount of power while providing high performance. Since these two design goals can conflict with each other, Altera devices and software tools allow designers to monitor and control the current with built-in architectural device features.

For example, MAX 7000 macrocells can be individually configured for high performance or low power during design entry. Turning the macrocell's Turbo Bit on allows the macrocell to function in a high-performance mode at the specified device ratings. If the Turbo Bit is turned off, the macrocell's built-in power-saving mode trades higher performance for lower current consumption.

Devices operating in low-power mode consume less current. The supply current (I_{CC}) can be reduced by as much as 50% depending on the design and operating frequency. Most Altera device data sheets provide a graph that shows the relationship between I_{CC} and frequency. For a device with the Turbo Bit option, the graph provides two ratios; one showing I_{CC} versus frequency when all macrocells have their Turbo Bits turned on, the other when all macrocells have the Turbo Bits off. Since most designs use a combination of Turbo and non-Turbo macrocells, a formula that accounts for this ratio and the frequency of operation is also provided with the graph. The values shown in the graph and formula are measured with no output loads and represent only the current necessary for device operation.

Thermal Analysis

A critical element of system reliability is the capacity of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat. Altera device packages are specifically designed to tolerate the worst-case conditions of most applications. However, in some applications, excessive device temperature may affect system reliability.

Thermal analysis should be completed early in the design process to help identify potential heat-related problems in the system and prevent the system from exceeding the device's maximum allowed junction temperature:

1. Estimate the maximum I_{CC} and maximum power for the application.
2. Calculate the maximum allowed power for the device and package.
3. Compare the estimated and allowed maximum power values.

In most applications, the power dissipated is significantly lower than the maximum allowed. However, this type of analysis should be perfomed for all projects. Several steps that can correct temperature-related problems are described later in this data sheet.

Estimating Maximum I_{CC} & Maximum Power

Use the following formula to estimate the maximum I_{CC}:

Estimated I_{CC} = no-load I_{CC} + DC_{OUT} + AC_{OUT}

The no-load I_{CC} can be obtained from the I_{CC}-versus-frequency graph provided in the device data sheet. Since this value is "unloaded," it is necessary to add the DC_{OUT} from steady-state outputs and the AC_{OUT} current from frequently switching outputs. DC_{OUT} depends on the number of steady-state outputs, the logic levels they drive, and the resistive load on each output. AC_{OUT} depends on the frequency at which each output switches and the capacitive load on each output.

The estimated I_{CC} is used together with the following formula to estimate the maximum power (P_{MAX}):

Estimated P_{MAX} = I_{CC} + $V_{CC\,MAX}$

☞ The actual I_{CC} should be measured after the project is completed to verify the maximum power estimate.

Calculating Maximum Allowed Power for the Device & Package

The following formula is used to calculate the maximum power allowed for a device:

$$\text{Allowed } P_{MAX} = \frac{150^\circ\,C - T_{AMB}}{\theta_{JA}} \quad or \quad P_{MAX} = \frac{150^\circ\,C - T_{CASE}}{\theta_{JC}}$$

The maximum allowable power is dependent on the maximum allowable junction temperature of the silicon, the ambient temperature of operation, and the package's thermal resistance (θ) when configured in the system. The maximum junction temperature is specified as 150° C. The ambient temperature depends on the application. The junction-to-ambient thermal resistance, θ_{JA}, is a measure of the worst-case thermal resistance for a device in still air, with convection cooling only. Forced-air flow or heat-sinking will increase the ability of a device to dissipate heat. The junction-to-case thermal resistance, θ_{JC}, is the lowest possible thermal resistance, representing a device with a large heat sink. The formula above uses θ_{JA} as a worst-case value. For systems that use a heat sink or forced-air cooling, some value between θ_{JA} and θ_{JC} is more appropriate. See Table 1.

Table 1. Thermal Resistance of MAX 7000 Devices

EPLD	Pin Count	Package	θ_{JA} (° C/W)	θ_{JC} (° C/W)
EPM7032	44	PLCC	52	9
		PQFP	C.F.	C.F.
		TQFP	C.F.	C.F.
EPM7032V	44	PLCC	C.F.	C.F.
		TQFP	C.F.	C.F.
EPM7064	68	PLCC	44	12
	84	PLCC	35	11
	100	PQFP	50	10
EPM7096	68	JLCC	48	12
		PLCC	44	12
	84	JLCC	30	C.F.
		PLCC	55	11
	100	CQFP	50	11
		PQFP	50	10
EPM7128	84	PLCC	35	11
	100	PQFP	C.F.	C.F.
	160	PQFP	40	7
EPM7160	84	PLCC	35	11
	100	PQFP	50	10
	160	PQFP	40	7
EPM7192	160	PGA	20	7
		PQFP	40	7
EPM7256	192	PGA	16	6
	208	CQFP	20	6
		MQFP	17	8

Note:
C.F. Consult Factory

Comparing Maximum Allowed Power & Estimated Maximum Power

To avoid reliability problems, the system designer should compare the values calculated for maximum allowed power and estimated maximum power. The estimated maximum power should be the smaller of the two values. If the estimated maximum power exceeds the maximum allowed power, refer to step 8 in "Preventing Heat Build-Up" later in this data sheet for suggestions on how to reduce power requirements for a design.

Preventing Heat Build-Up

The following steps list corrective actions to reduce the power, and thus reduce heat build-up for an application.

1. *Use available low-power features of the device.* Each MAX 7000 macrocell can be configured for low-power operation, with only a nominal increase in propagation delay, by turning the Turbo Bit off. All macrocells in the device that do not need to run in high-performance mode should be set to low-power mode.

2. *Choose a different device package.* A ceramic or higher pin-count package can be used. Ceramic packages dissipate more heat than plastic packages. Also, packages with higher pin counts can dissipate more heat through the connection to the PCB.

3. *Use forced-air cooling and/or heat-sinking.* Forced-air cooling improves the efficiency of convection cooling, reducing the surface temperature of the device. A heat sink connected to a device significantly increases heat dissipation by radiating heat via the metal mass.

4. *Slow the operation in portions of the circuit.* I_{CC} is proportional to the frequency of operation. Slowing parts of a circuit lowers the I_{CC} and hence reduces the power. Altera devices provide global or array clock sources for all registers. Signals that do not require high-speed operation can use a slower, array Clock that significantly reduces the system power consumption.

5. *Reduce the number of outputs.* DC and AC current is required to support all I/O pins on the device. Reducing the number of I/O pins may reduce the current necessary for the project, and thereby reduce the power.

6. *Reduce the amount of circuitry in the device.* Power depends on the amount of internal logic that switches at any given time. Reducing the amount of logic in a device reduces the current in the device. The same effect may be achieved by using a larger device, which also provides increased heat dissipation and maintains a single-device solution.

7. *Choose a different device family.* The MAX 7000 family provides more power-saving features than the MAX 5000 family. The Classic family provides power-saving features at low density.

8. *Modify the design to reduce power.* Identify areas in the design that can be revised to reduce the power requirements. Common solutions include reducing the number of switching nodes and/or required logic, and removing redundant or unnecessary signals. For assistance in locating less obvious changes, contact an Altera Applications engineer by calling (800) 800-EPLD.

Device Erasure

Altera Classic, MAX 5000/EPS464, and MAX 7000 devices use non-volatile, reprogrammable EPROM or EEPROM memory cells to retain the configuration data so that the configuration data does not need to be reloaded when the system powers up. EPROM and EEPROM memory-cell technologies have similar programming characteristics, but different erasure mechanisms.

Altera's EPROM-based devices (such as the MAX 5000/EPS464, EPM7256, and EPM7096 devices) are available in both plastic and ceramic packages. Plastic packages for EPROM devices are one-time-programmable devices; windowed ceramic packages allow erasure by exposure to UV light. Altera EPROM-based devices begin to erase when exposed to lights with wavelengths shorter than 4,000 Å. Since fluorescent lighting and sunlight fall into this range, an opaque label must be placed over the device window to ensure long-term reliability. To completely erase a device, it must be exposed to UV light with a wavelength of 2,537 Å. Devices should be erased for one hour by an eraser system with a power rating of 12,000 $\mu W/cm^2$. Altera devices may be damaged by long-term exposure to high-intensity UV light. Altera guarantees that devices can be programmed and erased at least 25 times, provided the recommended erasure exposure levels are used. Most devices can be reliably erased and reprogrammed many more times beyond this guaranteed minimum.

Altera's EEPROM-based devices (EPM7032, EPM7032V, EPM7064, EPM7128, EPM7160, EPM7192) are available in reprogrammable plastic packages. (Additionally, the EPM7192 is available in a windowless ceramic PGA package.) EEPROM cells are electrically erasable and therefore do not have an erasure window. These EEPROM-based devices are erased immediately before being programmed, and can be erased and reprogrammed up to 100 times.

MAX+PLUS II

Programmable Logic Development System & Software

February 1993, ver. 3 | Data Sheet

Introduction

Altera's fully integrated programmable logic development software, MAX+PLUS II, easily adapts to the designer's needs. MAX+PLUS II consists of a variety of modular applications centered around a logic compiler (see Figure 1). Applications and features can be added incrementally to tailor the design environment to the changing requirements of the designer.

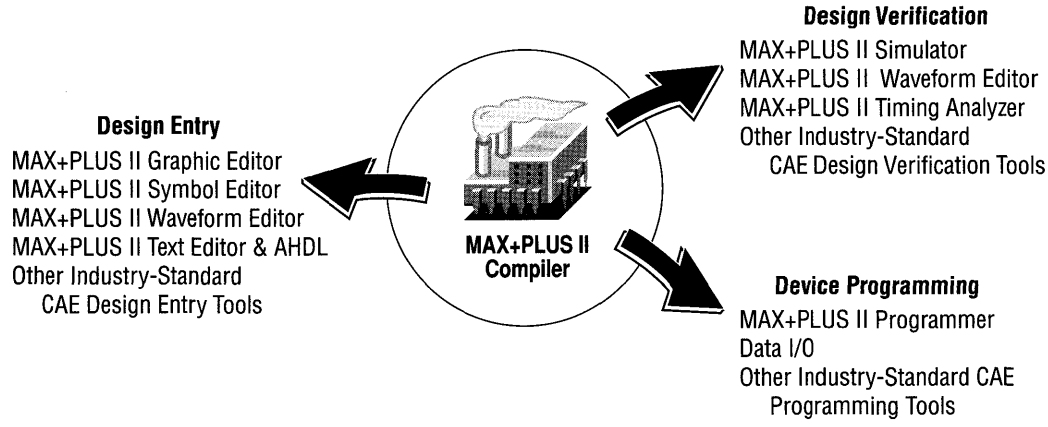
The MAX+PLUS II Compiler supports Altera's Classic, MAX 5000/EPS464, MAX 7000, and FLEX 8000 families of programmable logic devices, offering the industry's only truly architecture-independent programmable logic design environment. It provides powerful logic synthesis and minimization capabilities, efficiently fits designs with advanced algorithms, and creates standard data files for programming. In addition, the Compiler performs multi-device partitioning, which allows the designer to create fully integrated system-level functions.

MAX+PLUS II runs under Microsoft Windows on 386- or 486-based PCs and under X Windows on Sun SPARCstations and HP 9000 Series 700 workstations. On both the PC and workstation platforms, designs can be entered with the Altera Hardware Description Language (AHDL), as well as other industry-standard design entry tools. On the PC platform,

3 Products

Figure 1. MAX+PLUS II Compiler

The MAX+PLUS II Compiler is the core of the MAX+PLUS II development system, linking design entry with post-processing applications such as simulation, timing analysis, and programming.



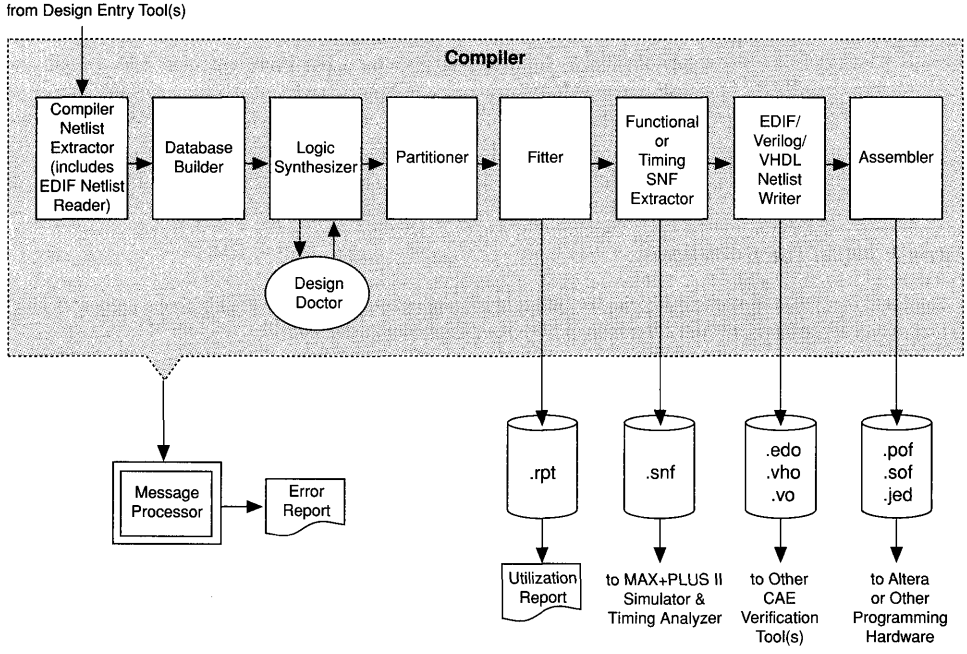
MAX+PLUS II offers a full set of highly integrated tools for every phase of design development, including the Graphic Editor for schematic capture, the Text Editor for text entry with AHDL, the Waveform Editor for designing and editing waveform-based designs, the Simulator for functional and timing simulation, the Timing Analyzer for timing verification, and the Programmer for programming Altera devices.

Regardless of the designer's preferred platform, MAX+PLUS II provides a rich graphical user interface, complemented by complete and instantly accessible on-line documentation. MAX+PLUS II provides a superior, easy-to-use desktop logic design environment that the designer can use exclusively or together with other industry-standard CAE tools.

Design Processing

The MAX+PLUS II Compiler consist of a series of modules and a design-rule checker that synthesize the logic, fit the project into one or more Altera devices, generate output files for simulating and programming, and check the project for errors. See Figure 2.

Figure 2. MAX+PLUS II Compiler Block Diagram



Compiler Netlist Extractor

The first module of the Compiler, the Compiler Netlist Extractor, extracts the netlist used to define the logic design. (A complete logic design is called a "project" in MAX+PLUS II. The project name is the same as the name of the top-level design file.) This module includes the EDIF Netlist Reader that converts standard EDIF 2 0 0 files into a MAX+PLUS II-compatible format. The Compiler Netlist Extractor checks the project for errors such as duplicate names or missing inputs. Errors are displayed by the Message Processor, which can be used to locate and highlight the errors in the appropriate design file. Most errors are detected and can be easily corrected at this stage of processing. A successfully extracted project is built into a database and passed to the Database Builder.

Database Builder

The Database Builder module creates a single, fully flattened database that integrates all files in the project hierarchy. It also examines the logical completeness and consistency of the project and checks for boundary connectivity and syntatical errors.

Logic Synthesizer

The Logic Synthesizer module supports both synthesized and what-you-see-is-what-you-get (WYSIWYG) design implementation. It can apply a number of algorithms that minimize and remove redundant logic to ensure that the logic cell structure is used as efficiently as possible for a specified device architecture. It also removes unused logic from the project.

Logic synthesis options help the designer guide the outcome of logic synthesis. Altera provides three "ready-made" synthesis styles, which specify the settings for multiple logic synthesis options. The designer can apply a style to set default synthesis options, create custom styles, or specify individual synthesis options on selected logic functions. These synthesis styles allow the designer to tailor synthesis options for a specific device family and thereby take advantage of that family's architecture. A number of advanced logic options further expand the designer's ability to influence logic synthesis.

Design Doctor

MAX+PLUS II also includes a design-rule-checker utility, appropriately called "Design Doctor." It checks each design file for logic that may cause reliability problems when the project in implemented in one or more devices. The user can choose one of three predefined sets of design rules, to specify how thorough design-rule checking should be, or create a custom set of rules.

Design rules are based on reliability guidelines that cover items such as asynchronous inputs, ripple Clocks, multi-level logic on Clocks, Preset and Clear configurations, and race conditions. Rule violations are explained to help the designer determine which edits are needed in the design files.

Partitioner

If a project does not fit into a single device, the Partitioner divides the project into multiple devices from the same device family. It attempts to split the project into the smallest possible number of devices while minimizing the number of pins used for inter-device communication.

Partitioning can be totally automatic, partially user-controlled, or fully user-controlled. If a project is too large to fit into a specified device, the designer can specify the type and number of additional devices.

Fitter

After partitioning, the Fitter applies heuristic rules to select the best possible implementation for the synthesized project in one or more devices. This automatic fitting relieves the designer of tedious place-and-route tasks. The Report File (**.rpt**), issued by the Fitter, shows project implementation as well as any unused resources in the device(s).

Timing & Functional SNF Extractor

The Timing SNF Extractor creates an optimized binary-format Simulator Netlist File (**.snf**) from the fully optimized project database generated by the Fitter. This timing SNF can be used by the MAX+PLUS II Simulator for timing simulation and by the MAX+PLUS II Timing Analyzer for full timing analysis. See "Design Verification" later in this data sheet.

The Functional SNF Extractor creates a functional SNF required for functional simulation. The Compiler generates this file before a project is synthesized; therefore, a functional SNF contains all nodes present in the original design files.

EDIF, Verilog & VHDL Netlist Writers

The EDIF, Verilog, and VHDL Netlist Writers create EDIF 2 0 0, Verilog, and VHDL netlists that contain all post-synthesis function and delay information for a completed project. Using Altera simulation libraries and conversion software, these files can be used with other standard design-verification tools from companies such as Cadence, Mentor Graphics, Synopsys, and Viewlogic. Interface software for industry-standard products from other CAE manufacturers is also available from Altera.

Assembler

The Assembler module creates one or more Programmer Object Files (**.pof**), SRAM Object Files (**.sof**), and/or JEDEC Files (**.jed**) for the compiled project. The MAX+PLUS II Programmer uses these files and standard Altera hardware to program the desired devices. Device programming is also available with other industry-standard programming equipment.

Design Entry

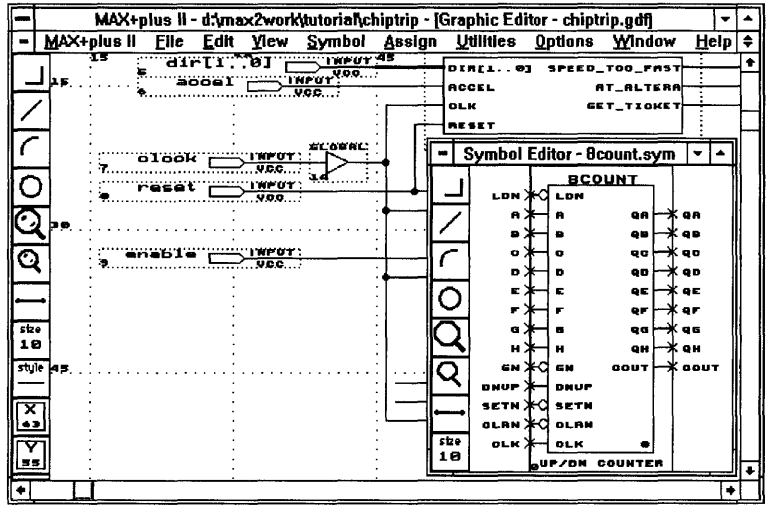
MAX+PLUS II can integrate design files generated with MAX+PLUS II or a variety of other industry-standard CAE design entry tools.

Graphic & Symbol Editors

The MAX+PLUS II Graphic Editor (shown in Figure 3) provides many features that make schematic entry fast and easy. Drag-and-drop editing quickly moves one or more objects or an entire area. During a move, a net can be preserved with the rubberbanding feature. The designer can also make a design more compact by connecting primitives with buses to create arrays of symbols. Over 300 74-series macrofunctions are available.

The high degree of integration between MAX+PLUS II applications allows information to flow freely to and from the Graphic Editor. For example, errors identified during compilation can be automatically located and highlighted in the schematic. If a project consists of two or more hierarchical levels, the designer can go from the Graphic Editor directly to all other design files in the hierarchy, regardless of whether they are graphic-, text-, or waveform-based.

Figure 3. MAX+PLUS II Graphic & Symbol Editors



MAX+PLUS II can automatically create a symbol for any design file. With the Symbol Editor (also shown in Figure 3), the designer can modify a symbol to customize its appearance, or create an entirely new symbol.

Text Editor

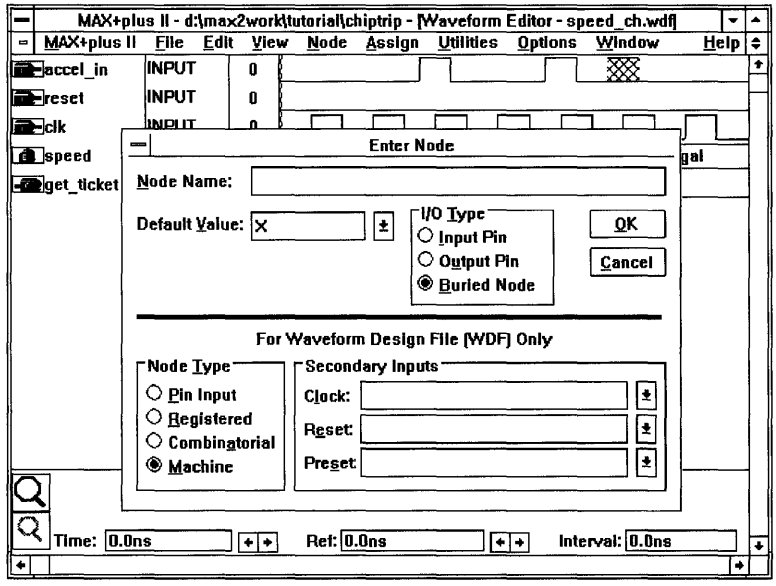
With the MAX+PLUS II Text Editor, the designer can view and edit any ASCII text file or any EDIF netlists created with other industry-standard CAE tools . The Text Editor is ideal for entering and editing design files in AHDL, which is fully integrated into the MAX+PLUS II system.

Waveform Editor

The MAX+PLUS II Waveform Editor (shown in Figure 4) is used to create and edit waveform design files, as well as input vectors for simulation and functional testing. The Waveform Editor also functions as a logic analyzer that allows the designer to view simulation results.

Waveform design entry is best suited for sequential and repeating functions. The Compiler's advanced waveform synthesis algorithms automatically generate logic from user-defined input and output waveforms that represent registered and combinatorial logic, as well as state machines. For state machines, the Compiler automatically assigns state bits and state variables.

Figure 4. MAX+PLUS II Waveform Editor



Waveform Editor features allow the designer to copy, cut, paste, repeat, and stretch functions; to work with internal nodes, flipflops, and state machines; to combine waveforms into groups that display binary, octal, decimal, or hexadecimal values; and to compare two sets of simulation results by superimposing one set of waveforms on another.

AHDL

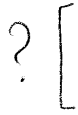
The Altera Hardware Description Language (AHDL) is a high-level modular language used to create logic designs for Altera devices. It can implement state machines, truth tables, conditional logic, and Boolean equations. AHDL syntax supports arithmetic and relational operations such as addition, subtraction, equality, and magnitude comparisons. Standard Boolean functions (e.g., AND, OR, NAND, NOR, XOR, and XNOR) are also available. Since AHDL supports groups, operations can be performed on a byte- or word-wide basis as well as on single variables. The designer can also use AHDL to assign logic to specific pins and logic cells within specific devices. Together, these features make it easy to implement complex projects in a concise, high-level description.

Industry-Standard CAE Design Entry Tools

The MAX+PLUS II Compiler can interface with other standard CAE tools that generate EDIF 2 0 0 netlist files. The Compiler's EDIF Netlist Reader uses Library Mapping Files (**.lmf**) to read the netlist files. These LMFs map function and pins from other CAE tools to MAX+PLUS II macrofunction and primitive names. Altera provides sample LMFs for over 100 74-series and custom macrofunctions for companies such Cadence, Intergraph (formerly DAZIX), Mentor Graphics, Minc, and Viewlogic. VHDL and Verilog design support is also available through Cadence, Mentor Graphics, and Synopsys. Exemplar design entry tools support AHDL design entry. For more information on other industry-standard design entry tools, see *CAE Software Support* in this data book.

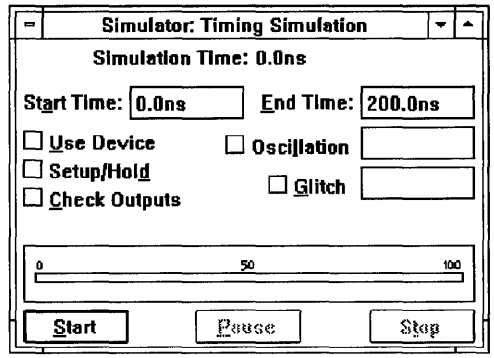
Design Verification

The MAX+PLUS II Simulator provides flexibility and control for modeling single- or multi-device projects. The Simulator uses the Simulator Netlist File (**.snf**) that is generated during compilation to perform functional and timing simulation for a project. See Figure 5.



The designer either defines input stimuli with a straightforward vector input language or draws waveforms directly with the MAX+PLUS II Waveform Editor. Simulation results can be viewed in the Waveform Editor or Text Editor and printed as waveform or text files.

Figure 5. MAX+PLUS II Simulator



The designer specifies commands either interactively or in a Command File (**.cmd**) to perform a variety of tasks, such as monitoring the project for glitches, oscillation, and register setup and hold time violations; halting the simulation when user-defined conditions are met; forcing flipflops high or low; and performing functional testing.

For easy comparison, the designer can superimpose the results of two simulations in the Waveform Editor.

Functional Simulation

The MAX+PLUS II Simulator supports functional simulation that tests the logical operation of a project before it is synthesized, allowing the designer to quickly identify and correct logical errors. The MAX+PLUS II Waveform Editor displays the results of functional simulation and provides easy access to all nodes in the project, including combinatorial functions.

Timing Simulation

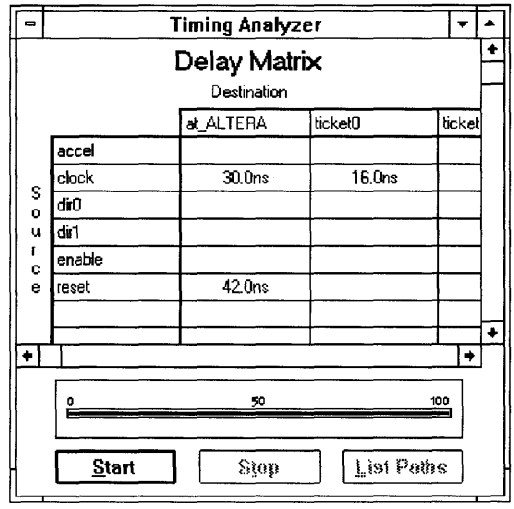
In a timing simulation, the MAX+PLUS II Simulator tests the project after it has been synthesized and optimized. Therefore, timing simulation simulates only those nodes that have not been eliminated during logic synthesis. The Simulator uses the SNF to perform timing simulation with 0.1-ns resolution.

If a setup or hold time, minimum pulse width, or oscillation period is violated, the Message Processor indicates where and when the problem occurred and locates the offending node in the original design file. The Waveform Editor then displays the time at which the problem occurred.

Timing Analysis

MAX+PLUS II includes powerful tools for analyzing the timing of a completed project. The designer simply tags start and end points in the Graphic, Text, or Waveform Editor or the Timing Analyzer to determine the shortest and longest propagation delays. The Timing Analyzer also determines setup and hold time requirements at device pins, as well as maximum Clock frequency. In addition, the Message Processor can locate critical paths identified by the Timing Analyzer in the design files for a project. See Figure 6.

Figure 6. MAX+PLUS II Timing Analyzer



Industry-Standard CAE Design Verification Tools

MAX+PLUS II generates standard EDIF and Verilog netlists that can be used in a variety of simulation environments, such as those provided by Cadence, Intergraph, Mentor Graphics, and Viewlogic. Logic Modeling SmartModels support all Altera devices and allow the designer to verify a circuit at both the chip and board level in different environments. For more information on other industry-standard CAE design verification tools, see *CAE Software Support* in this data book.

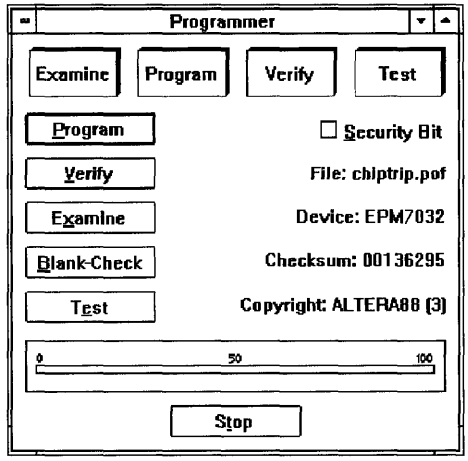
Device Programming

All hardware and software necessary for programming and verifying devices is available from Altera. The MAX+PLUS II Programmer uses POFs, SOFs, and JEDEC Files generated by the Compiler to program Altera devices. MAX+PLUS II can also generate Intel-format Hexadecimal Files (**.hex**) and Tabular Text Files (**.ttf**) for configuring FLEX 8000 devices.

The MAX+PLUS II Programmer allows the designer to program, verify, examine, blank-check, and functionally test devices. The programming hardware includes an add-on Logic Programmer card (for PC-AT, PS/2, or compatible computers) that drives the Altera Master Programming Unit (MPU). With the appropriate programming adapter, the MPU supports functional testing, so that vectors created for simulation can be applied to a programmed device to verify its functionality. The MPU also performs continuity checking to ensure adequate electrical contact between the programming adapter and the device. See Figure 7.

Programming support is also available from a large number of other programming hardware manufacturers. For more information, see *Programming Hardware Manufacturers* in this data book.

Figure 7. MAX+PLUS II Programmer



Software Maintenance Agreement

To guarantee timely upgrades to software and documentation, Altera offers a Software Maintenance Agreement that entitles the customer to software updates, discounts on optional software products, Applications Engineering support, and access to Altera's electronic bulletin board service (BBS).

Recommended System Configurations

To run MAX+PLUS II with optimum results, Altera recommends the following system configurations:

PC System Configuration

- ❑ 386- or 486-based PC-AT, PS/2 Model 70 or higher, or compatible computer
- ❑ 16 Mbytes of RAM
- ❑ DOS version 5.0 or higher
- ❑ Microsoft Windows version 3.1
- ❑ Microsoft Windows-compatible graphics card and monitor
- ❑ Approximately 30 Mbytes free disk space
- ❑ 1.44-Mbyte 3 ½-inch or 1.2-Mbyte, 5 ¼-inch floppy disk drive
- ❑ 2- or 3-button mouse compatible with Microsoft Windows 3.1
- ❑ Full-length 8-bit or Micro Channel Adapter slot for Logic Programmer card
- ❑ Parallel port

Sun Workstation System Configuration

- ❑ Sun SPARC2 workstation with color or monochrome monitor
- ❑ Sun OS 4.1.1 revision B or higher
- ❑ Sun OpenWindows 3.0
- ❑ 50 Mbytes free disk space
- ❑ 30 Mbytes of swap space
- ❑ Quarter-Inch Cartridge (QIC-24, 9 track) 60-Mbyte tape drive

Hewlett-Packard Workstation System Configuration

- ❑ HP 9000 Series 700 workstation with color or monochrome monitor
- ❑ HP-UX 8.07 or higher
- ❑ HP-VUE
- ❑ 50 Mbytes free disk space
- ❑ 30 Mbytes of swap space
- ❑ DDS-format tape drive

Ordering Information

For up-to-date information on available MAX+PLUS II software packages and development systems, refer to *Ordering Information* in this data book or contact Altera Marketing at (408) 894-7000.

Notes:

CAE Software Support

February 1993

Introduction

Altera recognizes the importance of supporting other established design tools, and works closely with leading CAE software manufacturers to provide high-quality, well-integrated support for Altera programmable logic devices. To ensure strategic partnerships with CAE tool manufacturers, Altera has established the ACCESS program. Through this program, Altera and its CAE partners either develop direct support for Altera devices or provide seamless integration with Altera's MAX+PLUS II development software.

Table 1 summarizes each company's design entry, compilation/synthesis, and simulation/verification products that support Altera devices directly or interface with MAX+PLUS II. As shown in Table 1, Altera also supplies design interface kits for several of the CAE tools. Altera recommends contacting CAE software manufacturers directly for details on their product features, specific device support, and product availability.

☞ Contact the Altera Applications Department by phone at (800) 800-EPLD or by fax at (408) 954-0348 for the most up-to-date information on CAE support.

Table 1. Standard CAE Support for Altera Devices (Part 1 of 2)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Accel Technologies, Inc. (619) 554-1000	Tango-PLD Tango-Schematic	✓ ✓	✓ ✓	✓ ✓
Acugen Software, Inc. (603) 891-1995	AADELAY AAMAX ATGEN			✓ ✓ ✓
Aldec, Inc. (805) 499-6867	Susie			✓
Cadence Design Systems, Inc. (408) 943-1234	Composer *(1)* Concept *(1)* PLD Option RapidSIM *(1)* SystemPLD Synergy Verilog, Verilog-XL *(1)* VHDL *(1)*	✓ ✓ ✓ ✓ ✓	 ✓ ✓ ✓ 	 ✓ ✓ ✓
Capilano Computing Systems, Ltd. (604) 669-6343	MacABEL	✓	✓	✓
Data I/O Corp. (800) 247-5700	ABEL-FPGA ABEL FutureNet	✓ ✓	✓ ✓ 	✓ ✓
Exemplar Logic, Inc. (510) 849-0937	CORE Solution		✓	
Flynn Systems Corp. (603) 891-1111	FS-High Density FS-PALibrary			✓ ✓
Intergraph Corp. (800) 239-4111	Aceplus AdvanSIM-1076 DLAB	✓ 	 	 ✓ ✓
ISDATA GmbH Germany: 0721/75 10 87	LOG/ic	✓	✓	✓
Logic Modeling Corp. (503) 690-6900	SmartModels			✓
Logical Devices, Inc. (800) 331-7766	CUPL	✓	✓	✓
Mentor Graphics Corp. (503) 626-7000	AutoLogic *(1)* Design Architect *(1)* PLD Synthesis QuickSim QuickSim II *(1)*	 ✓ 	✓ ✓ 	 ✓ ✓

Table 1. Standard CAE Support for Altera Devices (Part 2 of 2)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Minc Inc. (719) 590-1155	PGADesigner PLDesigner	✓ ✓	✓	✓
OrCAD Systems Corp. (503) 690-9881	PLD MOD SDT III VST	✓ ✓	✓	✓ ✓ ✓
Quad Design (800) 988-8250	Motive			✓
Quadtree Software Corp. (213) 597-5995	Designer's Choice Model			✓
Racal-Redac (201) 848-8000	Cadat System Expert Visula	✓	✓	✓
Synopsys, Inc. (415) 962-5000	Design Compiler *(1)*		✓	
Viewlogic Systems, Inc. (800) 422-4600	Viewdraw *(1)* ViewPLD Viewsim *(1)*	✓	 ✓	 ✓

Notes:

(1) Interface design kits are available from Altera.

Notes:

Programming Hardware Manufacturers

February 1993

Introduction

Table 1 lists the manufacturers of programming hardware that supports Altera devices. These companies are continually developing support for Altera programmable logic and configuration devices. Altera recommends contacting manufacturers directly for details on product features, specific device support, and product availability.

Table 1. Programming Hardware Manufacturers

Manufacturer	Telephone
Advantech	(408) 293-6786
Ando Electric Co., Ltd.	Japan: 011 81 3 3733 1161
Advin Systems Inc.	(408) 243-7000
Aval Data Corporation	Japan: 011 81 3 5375 7321
B&C Microsystems, Inc.	(408) 730-5511
BP Microsystems	(713) 461-9606
Bytek Corporation	(407) 994-3520
Caprilion Enterprise	Taiwan: 011 886 7 386 5061
Celectronic GmbH	Germany: 011 49 3041/36075
Data I/O	(206) 881-6444
Elan Digital Systems Limited, U.K.	0489 579799
ertec GmbH	Germany: 011 49 9131/75570
HAMIS Haase, Menrad & Co. GmbH	Germany: 011 49 531 79231
HI LO System/Tribal Research Co., Ltd.	Taiwan: 011 02 764 0215 6
ICE Technical Ltd.	Germany: 011 49 2267/67404
Logical Devices, Inc	(305) 974-0967
MicroPross	France: 011 33 20 47 90 40
Owen Electronic GmbH	Germany: 011 49 6381/5085
Prologic Systems	(303) 460-0103
SMS Micro Systems	(206) 883-8447
Stag Microsystems	(408) 988-1118
Sunrise Electronic Inc.	(818) 914-1926
System General	(408) 263-6667
Tribal Microsystems	(510) 623-8859
Xeltek	(408) 524-1934

Notes:

QFP Carrier & Development Socket

February 1993, ver. 3 | Data Sheet

Features

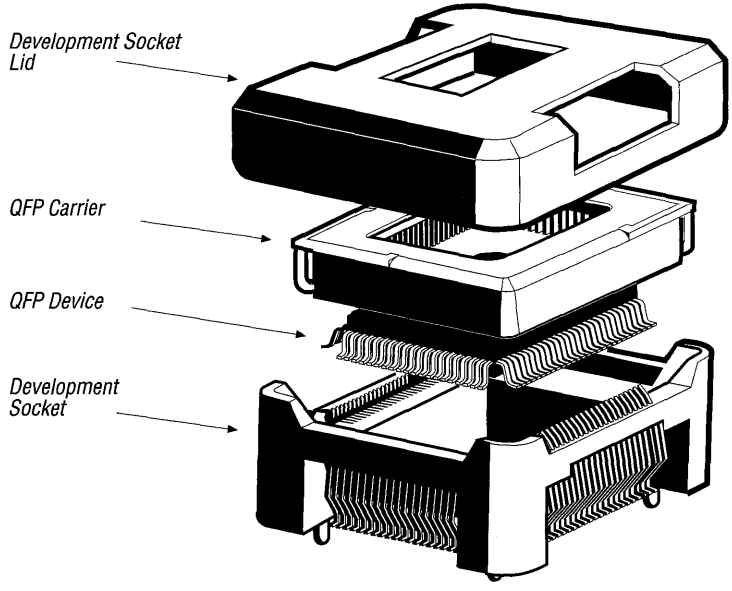
- Quad flat pack (QFP) carriers protect fragile leads on Altera QFP devices.
- Development socket allows on-board electrical and mechanical prototype testing with QFP packages.
- QFP carriers eliminate damage to leads caused by device handling.
- Carriers and sockets are available in 100-, 160-, and 208-pin counts.
- Development socket footprints match QFP footprints, making migration to production easier.

General Description

The Altera QFP carrier and development socket protect the fragile leads on QFP devices during shipping and throughout the development cycle. See Figure 1. The socket has the same lead footprint as the device, so it can be used both during mechanical and electrical prototyping.

The material used in the carrier and development socket helps prevent electrostatic damage to the devices while providing excellent AC circuit performance. QFP carriers and development sockets are currently available for 100-, 160-, and 208-pin QFP packages.

Figure 1. QFP Carrier & Development Socket



QFP Carrier

The carrier is a static-dissipative, molded plastic shell that holds the device and leads in a secure frame to prevent mechanical damage. The device is held in the carrier by recessed plastic clips.

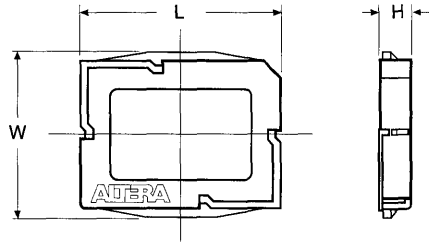
All MAX 5000/EPS464 and MAX 7000 QFP devices with 100 or more pins are shipped from the factory in carriers, thus eliminating the need to handle the delicate device leads. The carriers are packaged either in anti-static rails or strip packs. Devices can be programmed and erased while in the carrier. EPROM-based QFP devices are erased with a UV lamp; EEPROM-based QFP devices are erased in the programming adapter. Figure 2 shows the dimensions of the QFP carriers.

QFP devices without protective carriers should be handled with a vacuum wand at an electrostatically protected workplace to reduce the possibility of mechanical or electrical device damage.

Figure 2. QFP Carrier Dimensions

Dimensions are shown in millimeters.

Pin Count	L	W	H
100	25.2	21.2	4.2
160	33.2	35.2	5.1
208	33.2	35.2	5.1



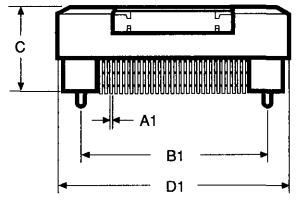
QFP Development Socket

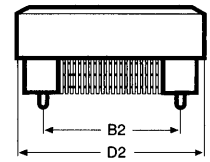
The QFP development socket has the same lead footprint as the QFP device. It ensures the device's electrical connection to the printed circuit board and provides excellent AC circuit performance: low noise, low capacitance, and low inductance. (A device mounted directly on the printed circuit board will provide better interconnect capacitance and inductance than a device loaded into the carrier/socket.) See Figure 3.

The development socket withstands the temperatures required by reflow technology. With the appropriate solder mask, multiple development sockets can be closely spaced on the board. Three alignment posts ensure correct orientation and provide sufficient registration for reflow soldering. When other components must be placed near the development socket, the designer must ensure that component leads do not conflict with the outline of the development socket.

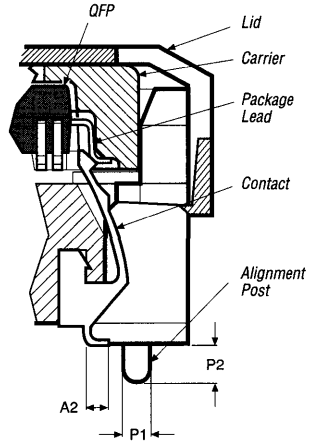
Figure 3. QFP Development Socket Dimensions

Dimensions are shown in millimeters.

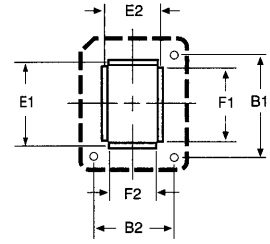




Contact & Lid Detail



Board Layout



Pin Count	A1	A2	B1	B2	C	D1	D2	E1	E2	F1	F2	P1	P2
100	0.20	0.60	25.0	19.0	12.0	31.20	25.30	22.70	16.70	30 Pads @ 0.65	30 Pads @ 0.65	1.0	1.5
160	0.20	0.60	33.8	33.8	12.8	39.60	39.60	31.15	31.15	40 Pads @ 0.65	40 Pads @ 0.65	1.0	1.5
208	0.20	0.60	33.8	33.8	12.8	39.60	39.60	30.75	30.75	52 Pads @ 0.50	52 Pads @ 0.50	1.0	1.5
Tolerance	±0.02	±0.12	±0.12	±0.12	±0.40	±0.20	±0.20	±0.12	±0.12			±0.03	±0.12

The QFP carrier is held in the development socket by the socket lid, which braces the carrier against the electrical contacts in the socket. These contacts connect the device leads to the development socket, ensuring a positive electrical connection that is not susceptible to mechanical interruption caused by jarring or impulsive shocks. The carrier design ensures that the pressure of the socket contacts does not significantly affect the coplanarity of the device leads.

This carrier/socket combination allows the designer to perform mechanical analysis during the functional prototyping cycle.

Step-by-Step Instructions

The following step-by-step instructions describe how to:

1. Insert the QFP carrier into the development socket
2. Remove the QFP carrier from the development socket
3. Program a device in the QFP carrier
4. Remove a device from the QFP carrier
5. Insert a device into the QFP carrier

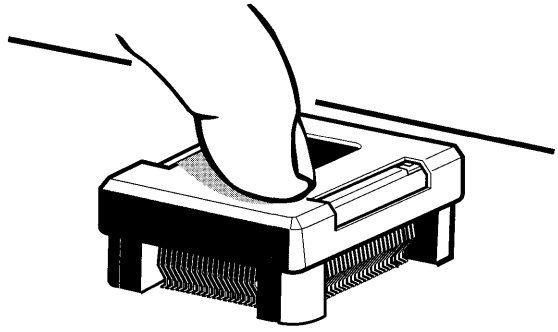
☞ Altera recommends removing the device from the QFP carrier only after it has been programmed and is ready to be soldered onto the board.

Inserting the QFP Carrier into the Development Socket

To insert the QFP carrier into the development socket:

1. Align the QFP carrier on the development socket by matching the beveled corner of the carrier to the beveled corner of the socket and aligning the alignment dots.
2. Place the socket lid over the socket and press down firmly on all four corners of the lid. See Figure 4.

Figure 4. Inserting the QFP Carrier into the Development Socket

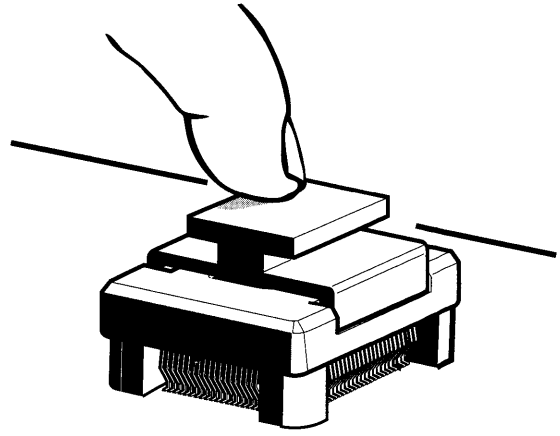


Removing the QFP Carrier from the Development Socket

To remove the QFP carrier from the development socket:

1. Place the extraction tool over the QFP socket lid, as shown in Figure 5.
2. Gently press down, making sure that the edges of the tool fit into the slots on the top of the lid. Two clicking sounds will be clearly audible.
3. While maintaining pressure, remove the lid and extraction tool together.
4. Remove the carrier.

Figure 5. Removing the QFP Carrier from the Development Socket



Programming Devices in the QFP Carrier

QFP devices that are shipped in the protective QFP carriers are ready to be programmed with the Altera Master Programming Unit (MPU) and the appropriate PLMQ-type programming adapter. With Altera programming software and hardware, test vectors can be directly applied to the device for programming verification and functional testing. Devices in QFP packages can also be programmed with industry-standard programming hardware from other manufacturers (e.g., Data I/O).

To program a device in the QFP carrier:

1. Place the QFP carrier with the device into the programming adapter, making sure that carrier and adapter are aligned correctly.
2. Close the retaining latch by pressing the latch against the socket. A clicking sound is clearly audible as the latch fastens over the socket.

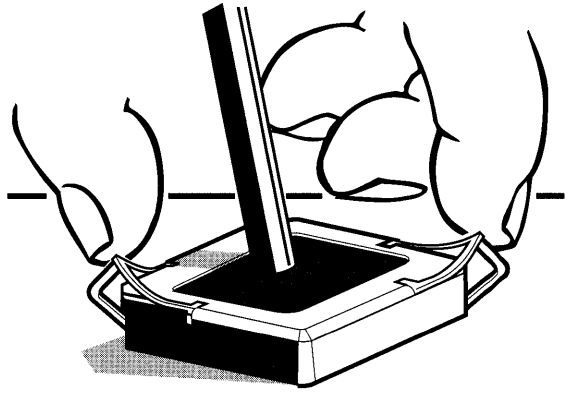
☞ The retaining latch on the clamshell-style programming adapter socket ensures good electrical contact between the device leads and the socket. The retaining latch must be shut after the QFP carrier is placed into the programming adapter; otherwise, programming problems may occur.

Removing a Device from the QFP Carrier

To remove a QFP device from the QFP carrier:

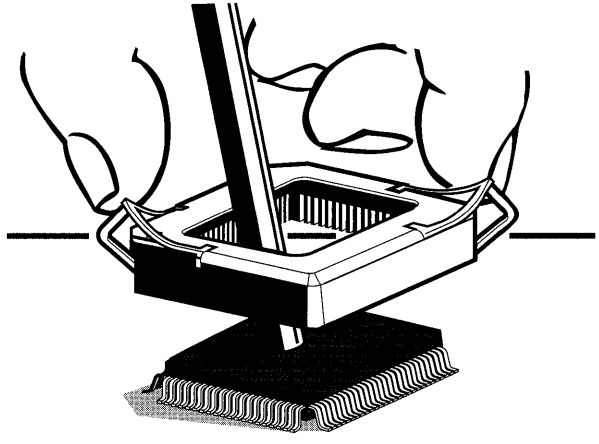
1. Place the QFP carrier against a flat surface.
2. Without applying pressure, hold down the device with the blunt end of a pencil or another similar tool.
3. Use thumb and forefinger to bend up the yellow retaining clips located on diagonal corners of the QFP carrier. See Figure 6.

Figure 6. Bending the Retaining Clips to Remove the QFP Device from the QFP Carrier



4. Lift the QFP carrier straight up. See Figure 7.

Figure 7. Lifting the QFP Carrier to Remove the QFP Device



Inserting a Device into the QFP Carrier

To insert a QFP device into the QFP carrier:

1. Hold the carrier bottom side up.
2. With thumb and forefinger, bend the yellow retaining clips outward.
3. Place the device into the carrier so that the device leads fit into the molded channels. The beveled corner of the device must be aligned with the beveled corner of the QFP carrier. When the device is securely seated in the carrier, the clips will snap back over the corners of the device and hold it in place.

The yellow plastic clips hold the device securely in place without hindering access to the leads. The open carrier top allows the EPROM-based QFP device to be placed under a UV lamp for device erasure.

☞ The QFP device should not be re-inserted into the QFP carrier once it has been removed.

Ordering Information

QFP carriers and development sockets are rated from –65° C to 155° C, and are qualified to handle commercial, industrial, and military operating temperatures. For up-to-date information on available QFP carriers and development sockets, refer to *Ordering Information* in this data book.

Notes:

Selecting Sockets for J-Lead Packages

February 1993, ver. 5 Application Brief 46

Introduction

Altera devices solve many of the problems designers face today. They offer low cost, low power, high reliability, and most importantly, high integration density. To further reduce the "real estate" demands of a system, many Altera devices are available in windowed ceramic and plastic J-lead chip carrier (JLCC/PLCC) packages.

J-lead packages are generally intended for surface-mount technology. However, surface-mount assembly places unique demands on the development and manufacturing processes by requiring different CAD symbols for printed circuit board (PCB) layout, different test and reliability procedures for buried vias within PCBs, and a different soldering process for production (vapor phase versus wave solder). Bonding devices to a PCB also removes the possibility of convenient erasure and reprogramming, which are particularly important during development.

A popular compromise that preserves the advantages of J-lead packages without the surface-mount process requirements is to socket the J-lead device. The socket can then be mounted using conventional techniques such as through-hole soldering to a PCB or mounting in a socketed carrier board for wire wrap.

This application brief discusses the following topics:

- Types of sockets available for J-lead devices
- Criteria for selecting burn-in or production sockets
- Results of Altera's evaluation of 44-, 68-, and 84-pin production sockets for use with windowed ceramic J-lead devices
- Carrier boards for use with wire-wrap panels and J-lead packages

☞ Information in this application brief is based on tests performed by Altera and information provided to Altera by various vendors, and is believed to be accurate. Altera assumes no liability for the use of third-party products mentioned in this publication.

Mechanical Considerations

There are two distinct types of sockets: burn-in and production sockets. Burn-in sockets are zero-insertion-force sockets. Since they will not deform the device pins, burn-in sockets are the preferred device carrier during the prototyping phase of a design. Newer burn-in sockets are also available with dimensions similar to those of production sockets.

Altera strongly recommends using a burn-in socket during the development and prototype phases of a project. Lower-cost production sockets should be used only after the design enters the production phase. Production sockets, designed to hold a device permanently and securely, exert force on the device pins. After several insertions, this force can deform the pins and eventually cause them to short out or fail to make contact.

Production sockets must be chosen carefully. If the device needs to be removed many times for reprogramming, low-insertion-force sockets that will not significantly deform the device pins for as many as 10 insertions are preferable. For high-stress environments (e.g., strong G-forces, thermal shock, high humidity), sockets with high insertion forces and optional retention clips are available. To further reduce the possibility of deforming device pins, most manufacturers of high-quality sockets include a stand-off inside the socket that prevents a device from being forced too far into a socket and having its pins bent.

Socket Evaluation

Altera tested production sockets from several manufacturers for use with 44-, 68-, and 84-pin windowed ceramic J-lead devices. Each socket underwent three tests:

- The change in the gap between the corner pins of each device was measured before and after each of 10 insertions.
- Each pin of the socket was wired in series and tested for open or short circuits lasting longer than 10 µs. This opens-and-shorts test was performed while the socket was attached to a vibration block. The amplitude of vibration was 3.0 mm peak-to-peak at a frequency that varied from 10 Hz to 55 Hz to 10 Hz, in 1-minute cycles for 2 hours. The vibration test was performed on all three axes at 70° C.
- The actual point of contact between the socket pin and the device lead was photographed to determine the direction of the forces between them and the amount of surface contact.

Table 1 shows the results of the opens-and-shorts tests for the 44-, 68-, and 84-pin production sockets that passed the tests. Ranking was determined by the socket's ability to maintain the device's pin integrity after multiple device insertions. For more information about these socket tests, call Altera Applications at (800) 800-EPLD.

Vendors may provide additional information about their products, such as material selection, prevention of solder ingress during wave soldering, or lead shape. Altera recommends qualifying sockets before committing to a particular vendor.

Table 1. Summary of Production Socket Analysis

Pin Count	Vendor & Part Number	Comments
44	Augat Inc. PCS-044A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
	AMP, Inc. 821575-1	Large pin deformation. Contact force has a downward component. No retainer clip option.
68	Augat Inc. PCS-068A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
	ITT/Cannon Corporation LCS-68-2	Low pin deformation. Contact force has a downward component. Retainer clip option.
	3M/Textool Corporation 2-0068-06234-070-038-077	Moderate pin deformation. Contact force is lateral. Retainer clip option.
	AMP, Inc. 821574-1	Moderate pin deformation. Contact force has a downward component. Retainer clip option.
84	Augat Inc. PCS-084A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
	ITT/Cannon Corporation LCS-84-2	Moderate pin deformation. Contact force has a downward component. Retainer clip option.
	Burndy Corp. QILE84P-410T	Large pin deformation. Very tight fit. No retainer clip option.
	AMP, Inc. 821573-1	Large pin deformation. Very tight fit. No retainer clip option.

Table 2 shows the contact distance for Altera's windowed ceramic and plastic J-lead (JLCC and PLCC) device packages. These measurements should be used to select a socket (preferably with internal stand-offs) for use with Altera devices.

Table 2. Device Contact Distances

Pin Count	Device Package	Contact Distance (mils)	
		Minimum	Maximum
20	PLCC	385	395
28	JLCC, PLCC	485	495
44	JLCC, PLCC	685	695
68	JLCC, PLCC	985	995
84	JLCC	1180	1200
	PLCC	1185	1195

Packaging Options for Wire-Wrap Applications

Wire-wrap applications require a through-hole mount compatible with the J-lead package. The sockets specified do not typically conform mechanically to most wire-wrap panels. Wire-wrap cards have machine receptacles in rows with 100-mil spacing between receptacles and 300-mil spacing between rows.

Carrier boards provide an effective way to bridge the gap. Mounting a socket to a carrier board provides the convenience of wire wrap with only a small real estate penalty. Some carrier boards have signal routing with shorter paths or 45-degree bends to minimize signal reflection.

Manufacturers

Table 3 lists corporate offices of the vendors noted in this application brief. Contact the appropriate vendor for additional information.

Table 3. Manufacturers of J-Lead Sockets

Product	Company	Telephone Number
Production Sockets	3M/Textool Corp.	(800) 225-5373
	AMP, Inc.	(800) 522-6752
	Augat Inc.	(508) 699-9800
	Burndy Corp.	(408) 245-2590
	ITT/Cannon Corp.	(714) 261-5300
Test & Burn-In Sockets	3M/Textool Corp.	(800) 225-5373
	AMP, Inc.	(800) 522-6752
	Advanced Interconnections Corp.	(401) 823-5200
	Dai-Ichi Seiko Co., Ltd.	Japan: 011 81 0482 53 3131
	Emulation Technology, Inc.	(408) 982-0660
Carrier Boards & Wire-Wrap Adapters	Advanced Interconnections Corp.	(401) 823-5200
	Emulation Technology, Inc.	(408) 982-0660

Altera Device Package Outlines

February 1993, ver. 3

Introduction

This data sheet provides package outlines for all Altera MAX 7000 devices. Table 1 shows the type of packages, lead materials, and lead finishes available.

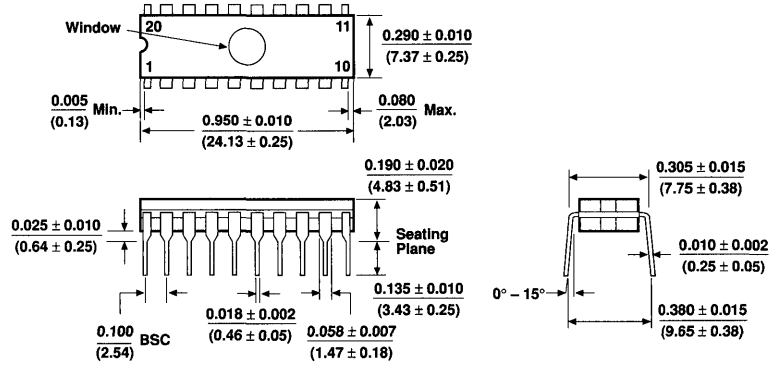
Table 1. EPLD Packages

Package Type	Package Code	Lead Material	Lead Finish
Ceramic dual in-line	D	Alloy 42	Solder dip
Plastic dual in-line	P	Copper	Solder dip (60/40)
Ceramic J-lead chip carrier	J	Alloy 42	Solder dip (60/40)
Plastic J-lead chip carrier	L	Copper	Solder plate (80/20)
Ceramic pin-grid array	G	Alloy 42	Gold over nickel plate
Plastic small-outline IC	S	Copper	Solder plate (80/20)
Ceramic quad flat pack	W	Alloy 42	Matte tin plate
Plastic quad flat pack	Q	Copper	Solder plate (80/20)
Metal quad flat pack	M	Copper	Solder plate (80/20)
Plastic thin quad flat pack	T	Copper	Solder plate (80/20)

Package outlines are listed here in ascending size order. The dimensions shown are nominal with a tolerance of 0.020 in. (0.51 mm) unless otherwise indicated. Maximum lead coplanarity is 0.004 in. (0.10 mm). For information on device package ordering codes, see *Ordering Information* in this data book.

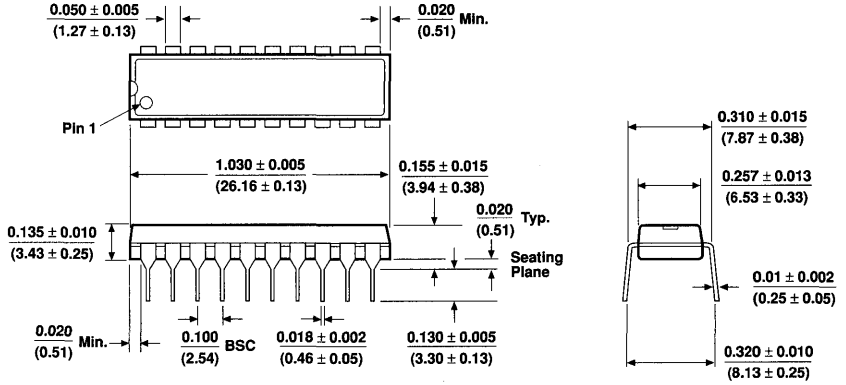
20-Pin Ceramic Dual In-Line Package (CerDIP)

Dimensions are shown in inches/(millimeters). For military-qualified product, see case outline in MIL-STD-1835.



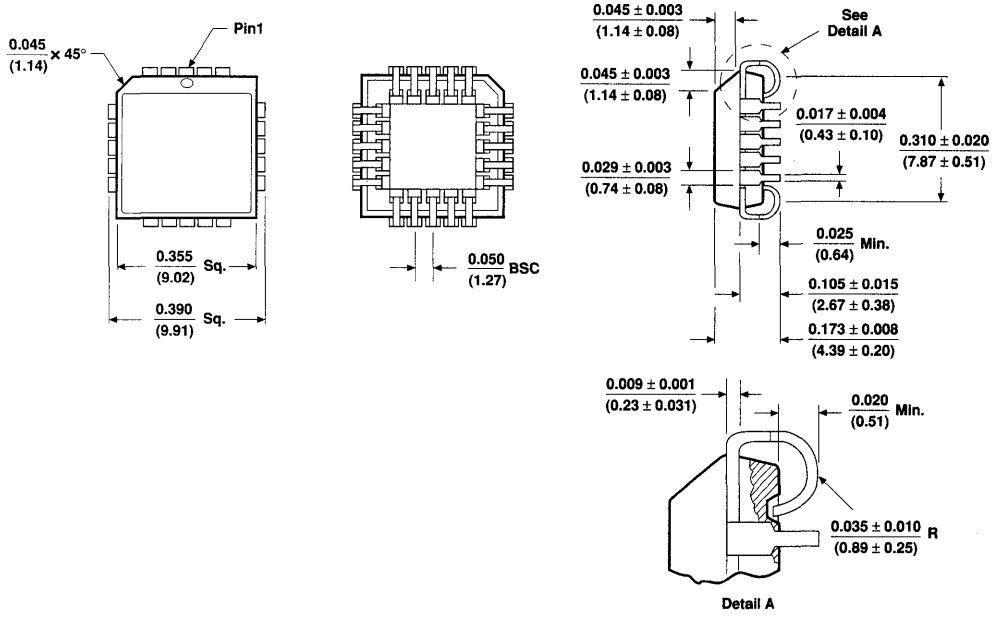
20-Pin Plastic Dual In-Line Package (PDIP)

Dimensions are shown in inches/(millimeters).



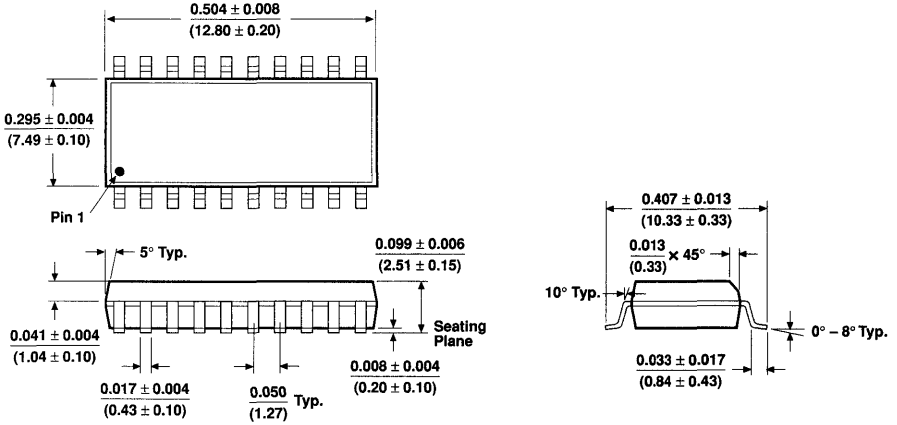
20-Pin Plastic J-Lead Chip Carrier (PLCC)

Dimensions are shown in inches/(millimeters).



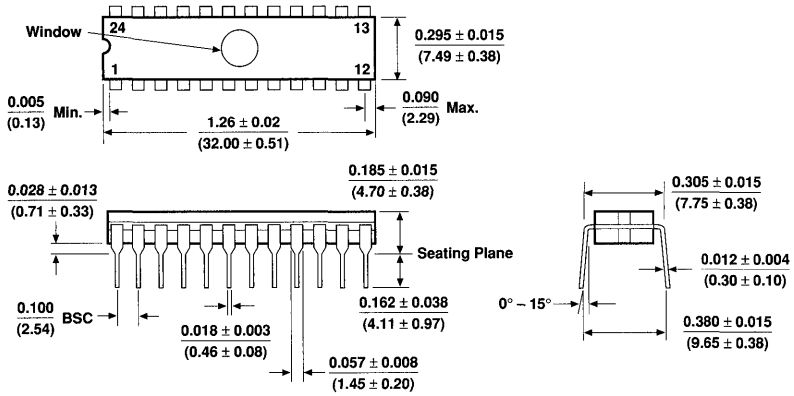
20-Pin Plastic Small-Outline IC (SOIC)

Dimensions are shown in inches/(millimeters).



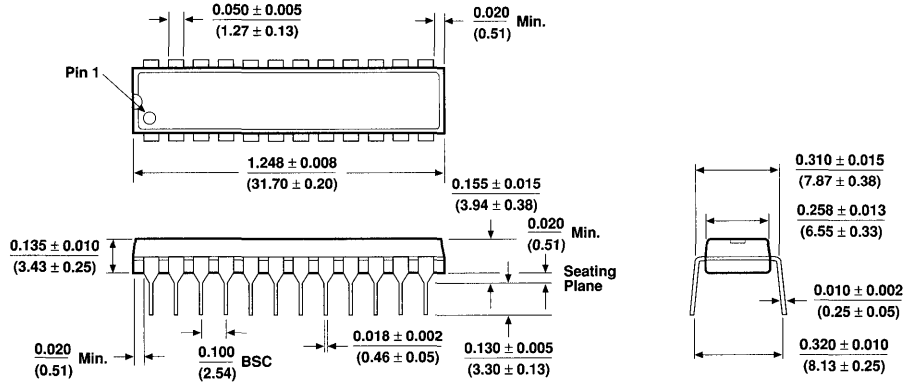
24-Pin Ceramic Dual In-Line Package (CerDIP)

Dimensions are shown in inches/(millimeters). For military-qualified product, see case outline in MIL-STD-1835.



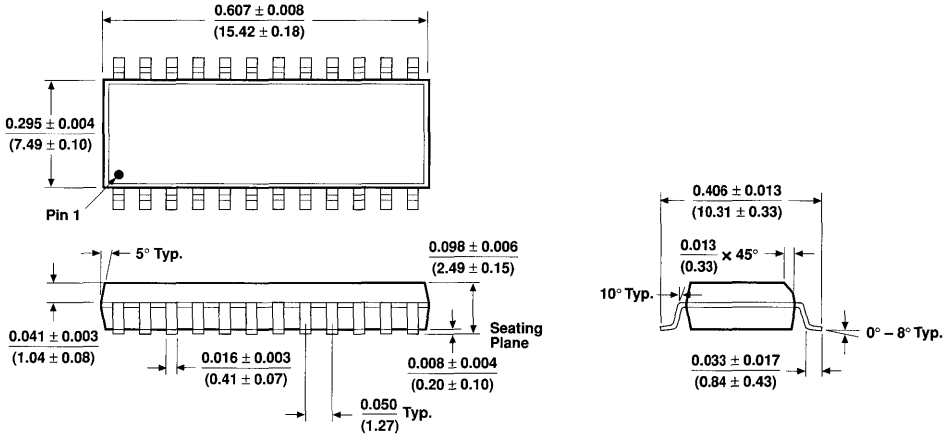
24-Pin Plastic Dual In-Line Package (PDIP)

Dimensions are shown in inches/(millimeters).



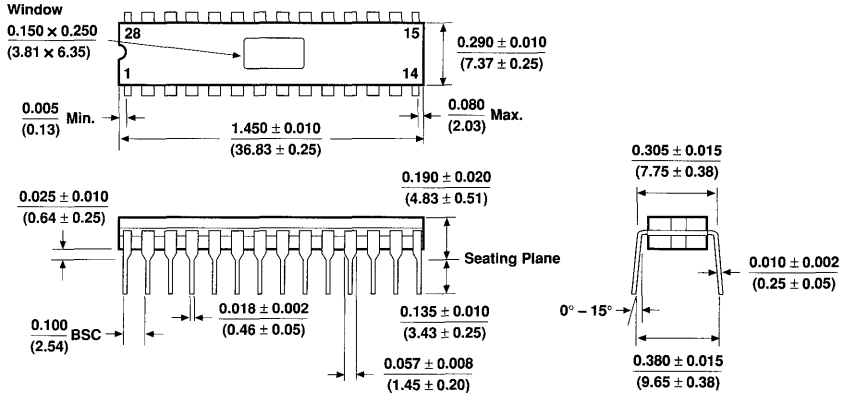
24-Pin Plastic Small-Outline IC (SOIC)

Dimensions are shown in inches/(millimeters).



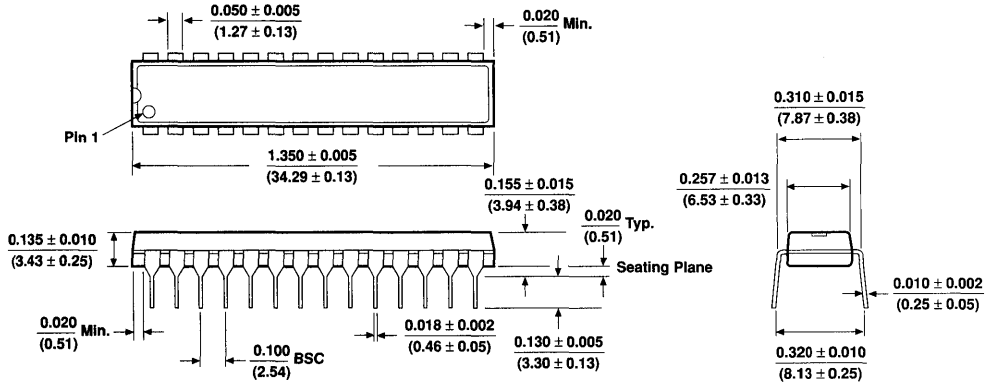
28-Pin Ceramic Dual In-Line Package (CerDIP)

Dimensions are shown in inches/(millimeters).



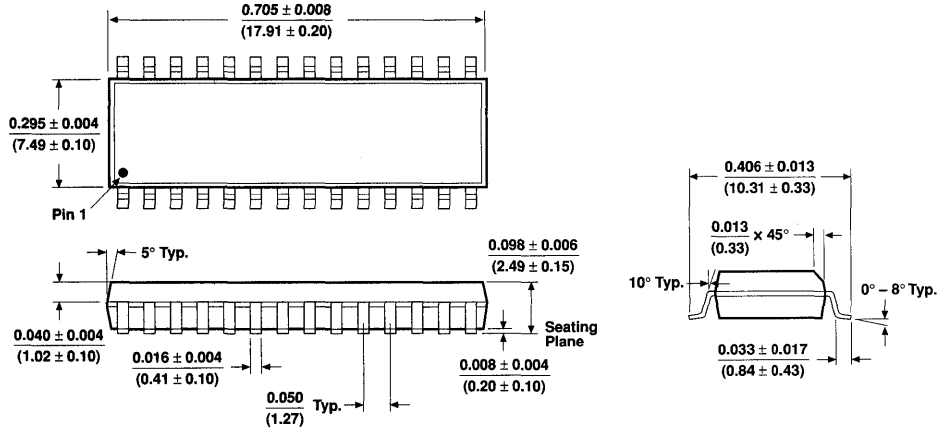
28-Pin Plastic Dual In-Line Package (PDIP)

Dimensions are shown in inches/(millimeters).



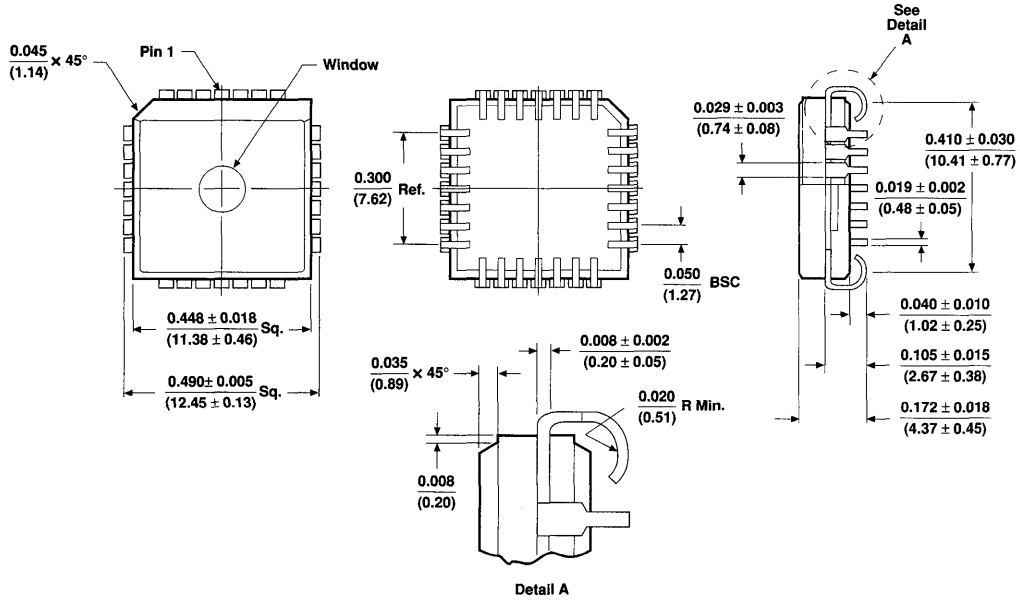
28-Pin Plastic Small-Outline IC (SOIC)

Dimensions are shown in inches/(millimeters).



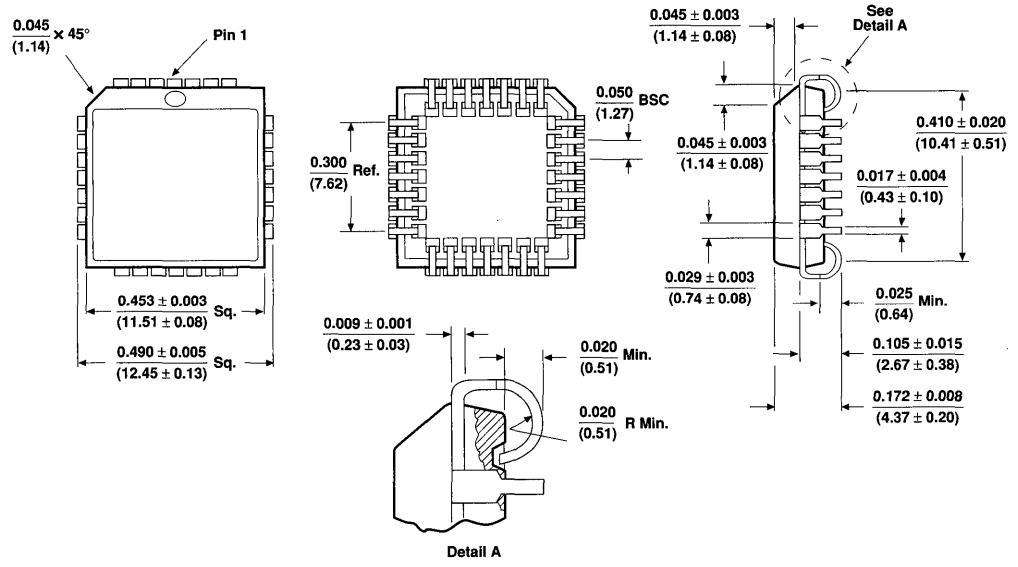
28-Pin Ceramic J-Lead Chip Carrier (JLCC)

Dimensions are shown in inches/(millimeters). For military-qualified product, see case outline in Altera Military Product Drawing 02D-00194.



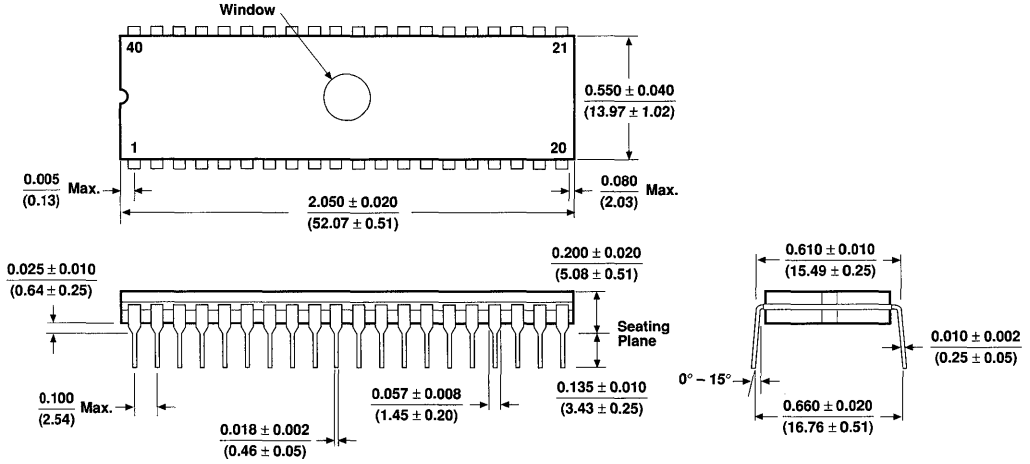
28-Pin Plastic J-Lead Chip Carrier (PLCC)

Dimensions are shown in inches/(millimeters).



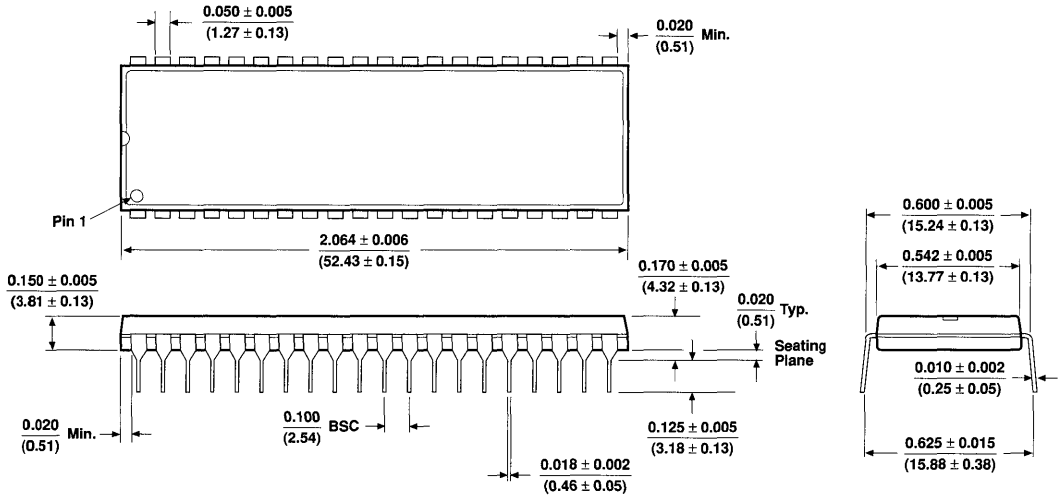
40-Pin Ceramic Dual In-Line Package (CerDIP)

Dimensions are shown in inches/(millimeters). For military-qualified product, see case outline in MIL-STD-1835.



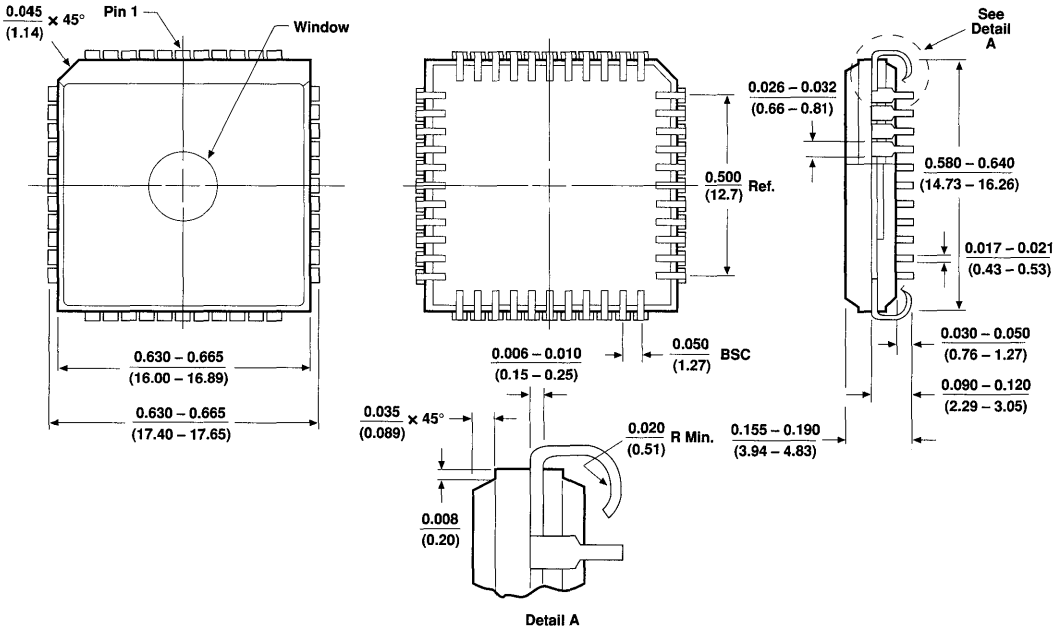
40-Pin Plastic Dual In-Line Package (PDIP)

Dimensions are shown in inches/(millimeters).



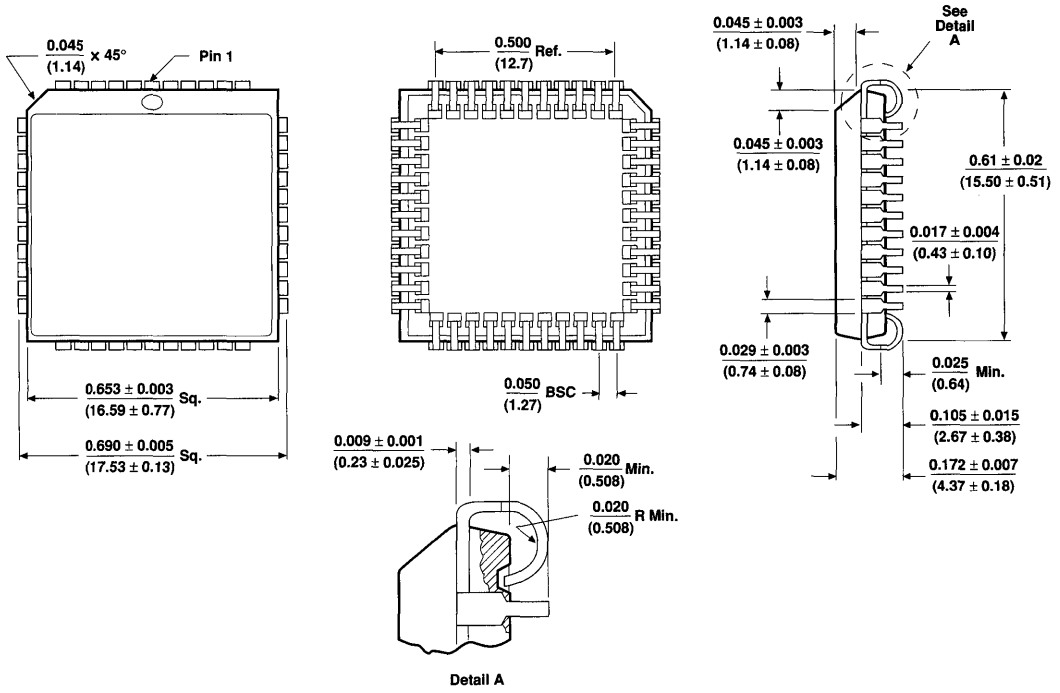
44-Pin Ceramic J-Lead Chip Carrier (JLCC)

Dimensions are shown in inches/(millimeters). Where appropriate, a minimum-to-maximum range is shown. For military-qualified product, see case outline in MIL-STD-1835.



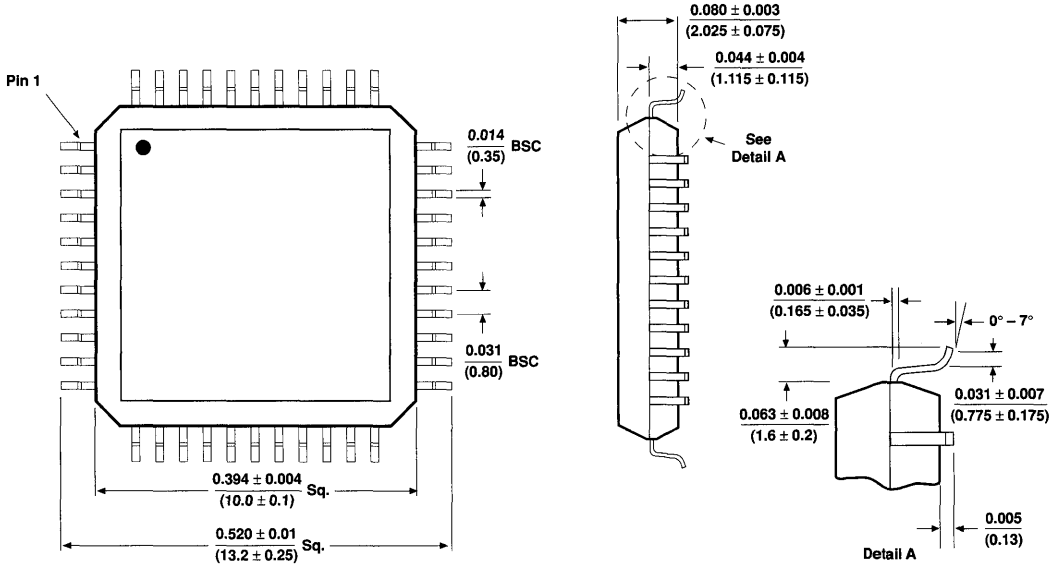
44-Pin Plastic J-Lead Chip Carrier (PLCC)

Dimensions are shown in inches/(millimeters).



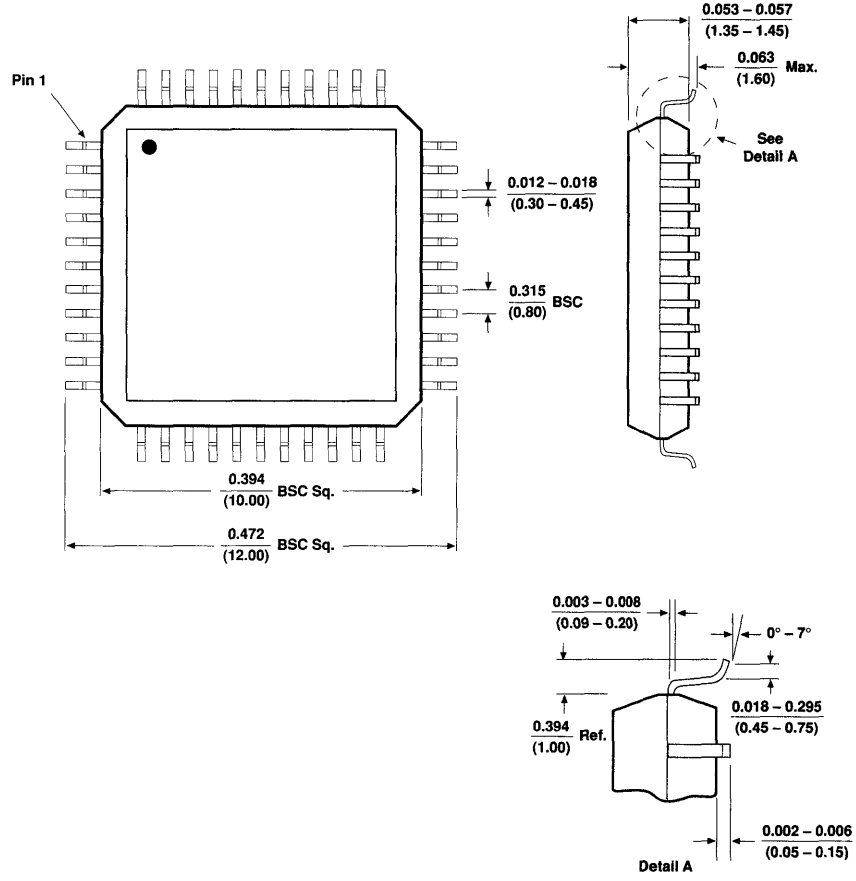
44-Pin Plastic Quad Flat Pack (PQFP)

Dimensions are shown in inches/(millimeters).



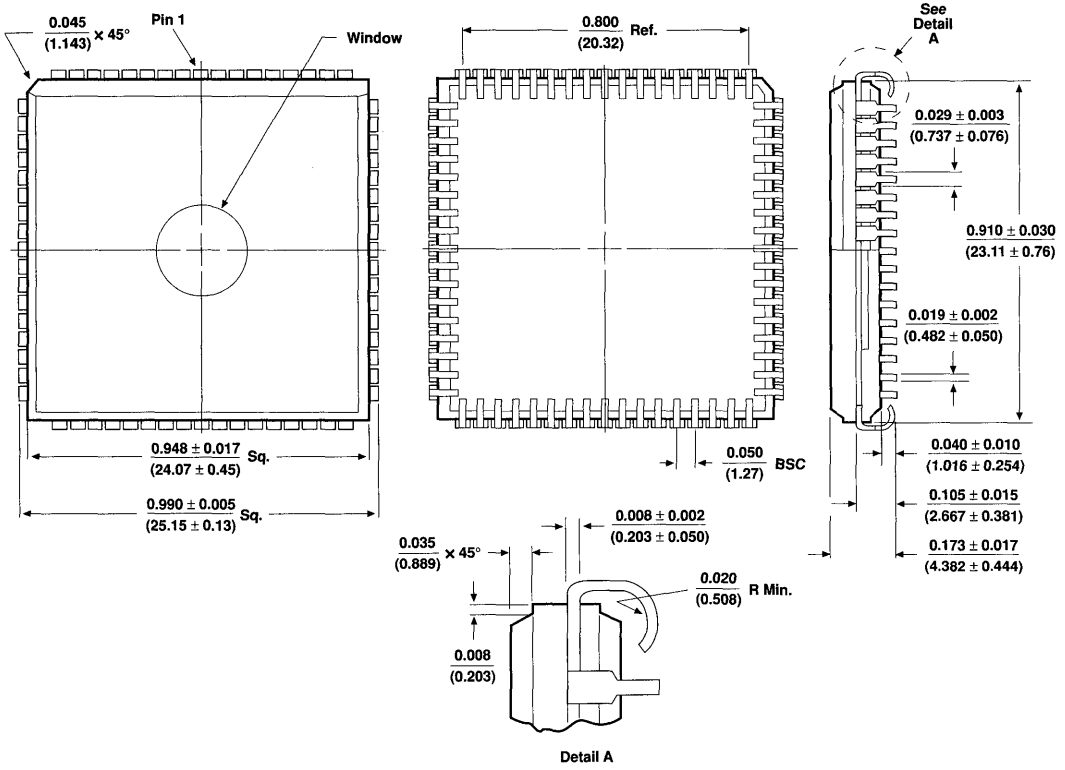
44-Pin Thin Plastic Quad Flat Pack (TQFP)

Dimensions are shown in inches/(millimeters). Where appropriate, a minimum-to-maximum range is shown.



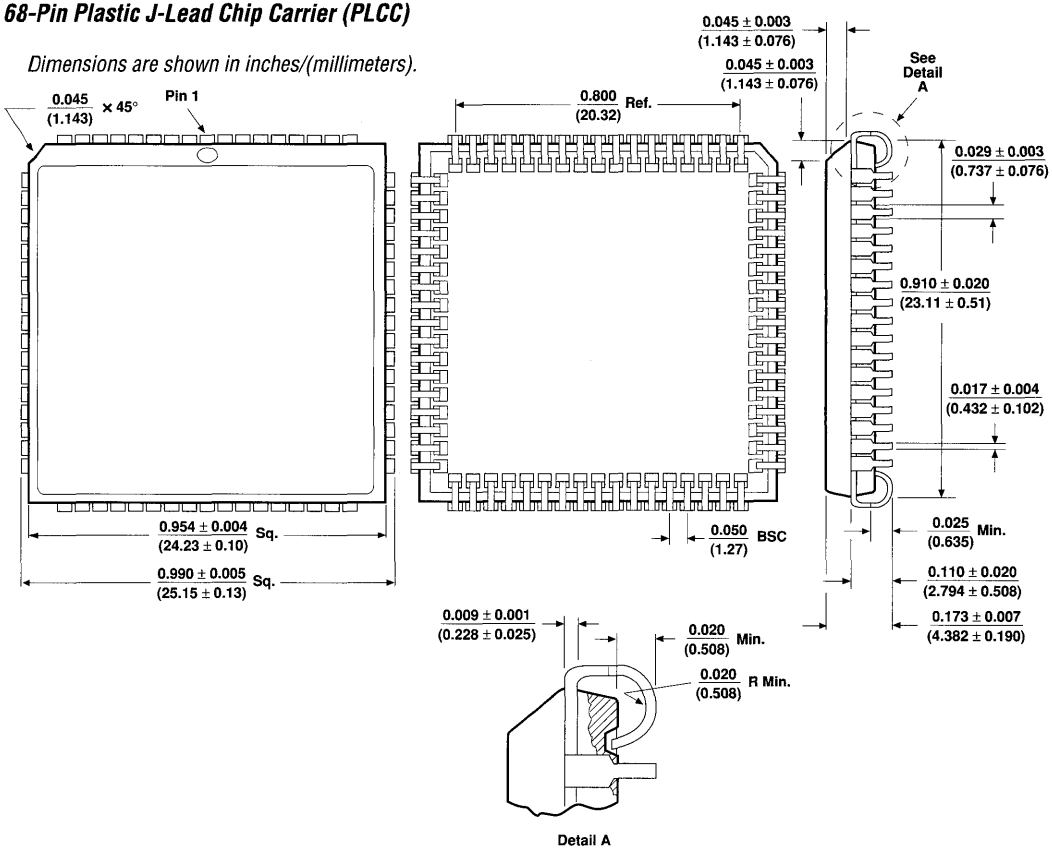
68-Pin Ceramic J-Lead Chip Carrier (JLCC)

Dimensions are shown in inches/(millimeters). For military-qualified product, see case outline C-J2 in Appendix C of MIL-M-38510.



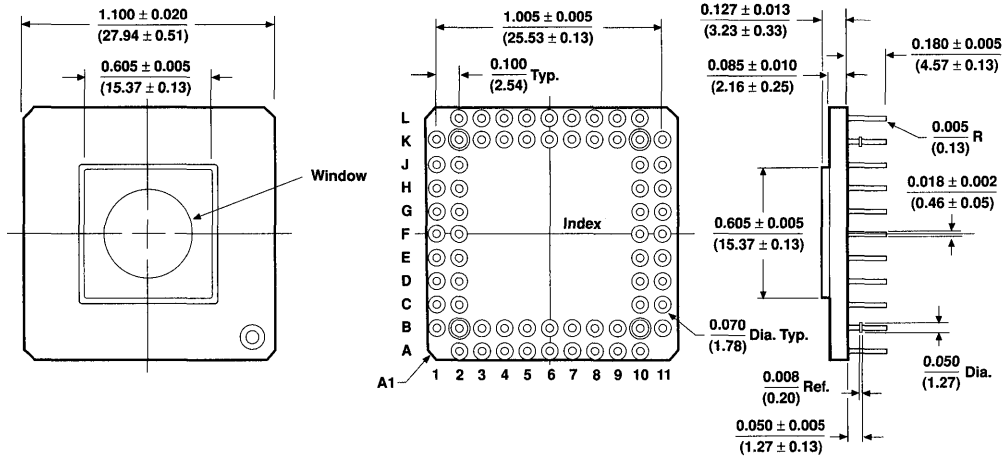
68-Pin Plastic J-Lead Chip Carrier (PLCC)

Dimensions are shown in inches/(millimeters).



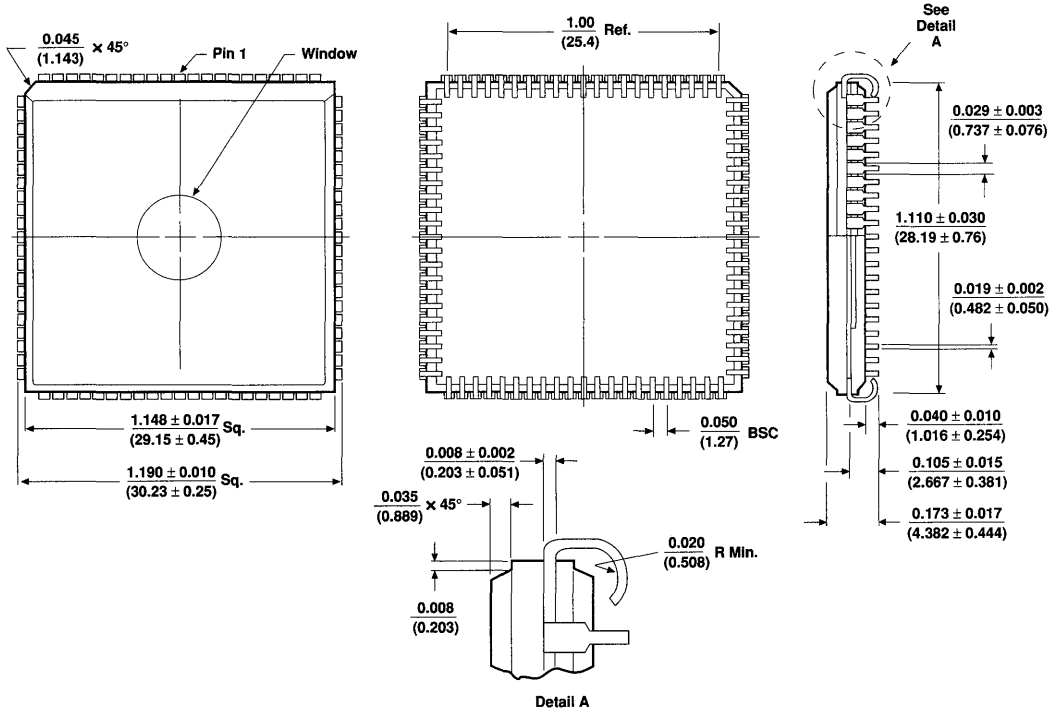
68-Pin Ceramic Pin-Grid Array (PGA)

Dimensions are shown in inches/(millimeters). For military-qualified product, see case outline in Altera Military Product Drawing 02D-00205.



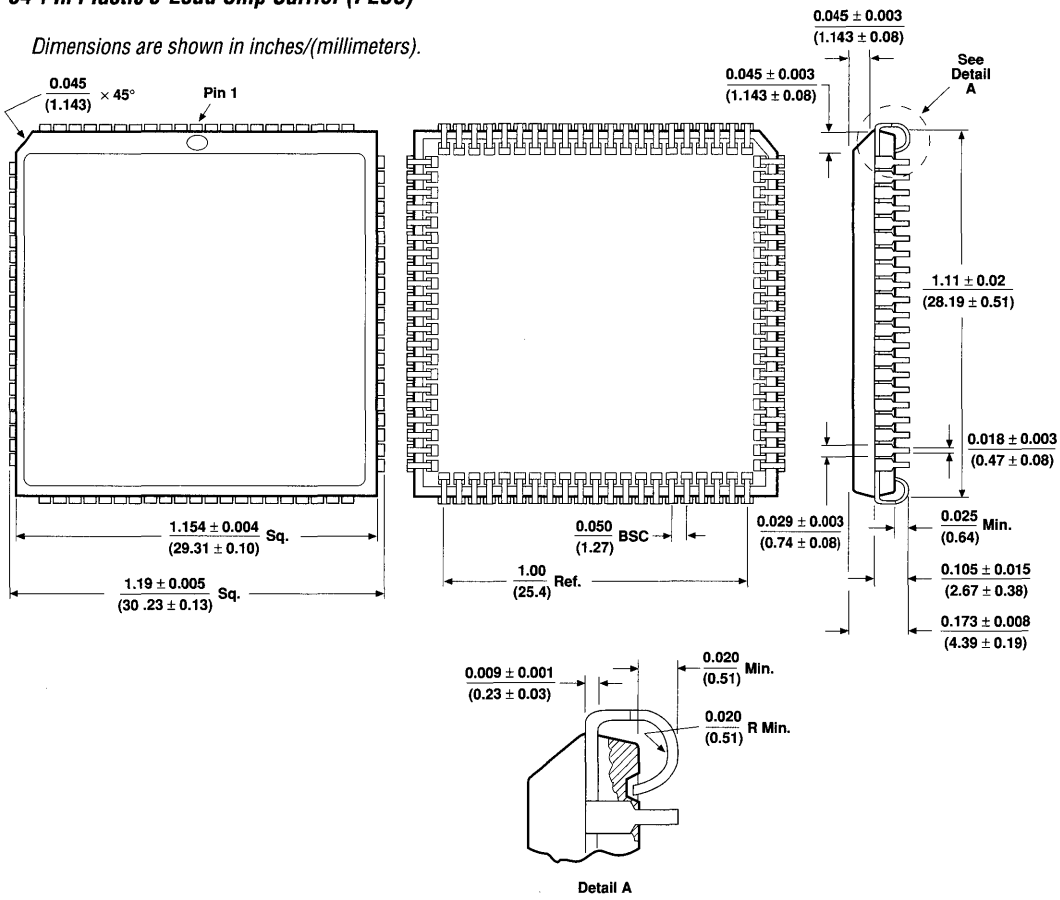
84-Pin Ceramic J-Lead Chip Carrier (JLCC)

Dimensions are shown in inches/(millimeters).



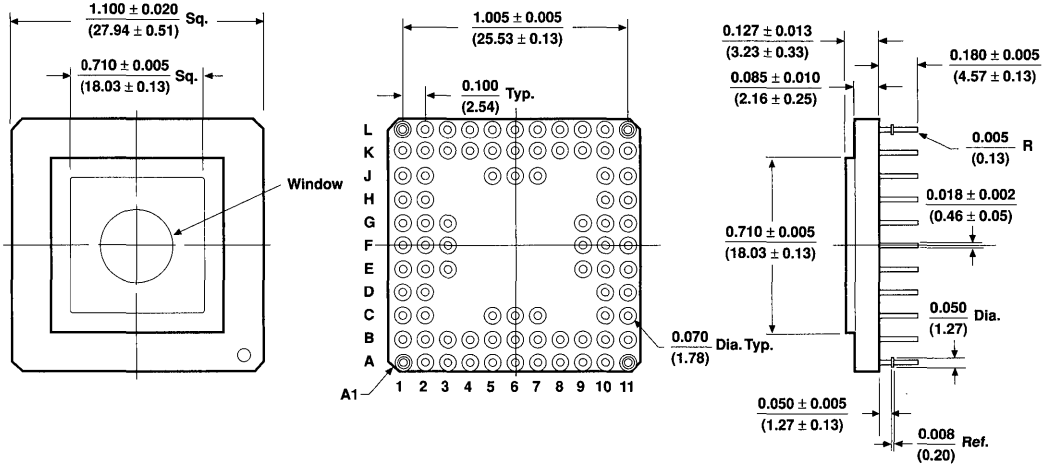
84-Pin Plastic J-Lead Chip Carrier (PLCC)

Dimensions are shown in inches/(millimeters).



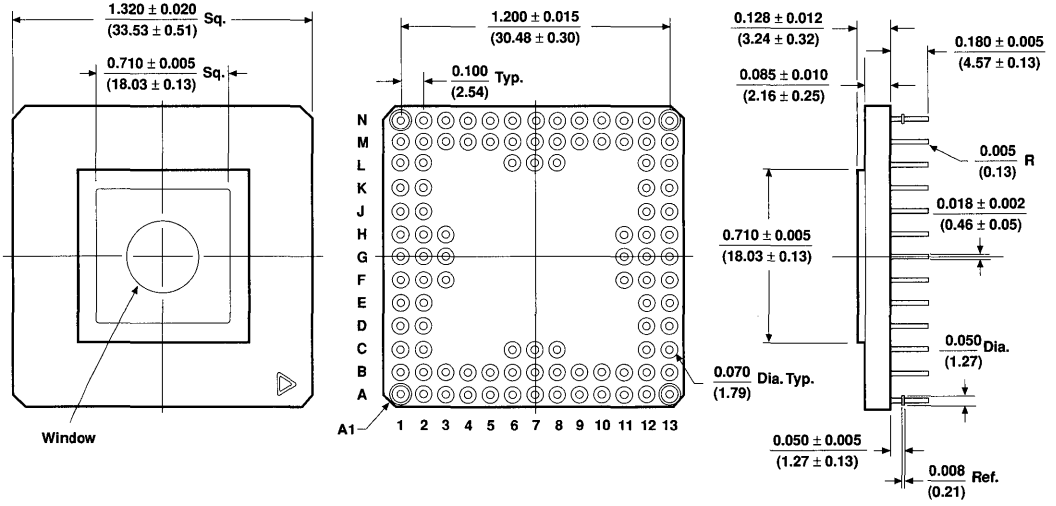
84-Pin Ceramic Pin-Grid Array (PGA)

Dimensions are shown in inches/(millimeters).



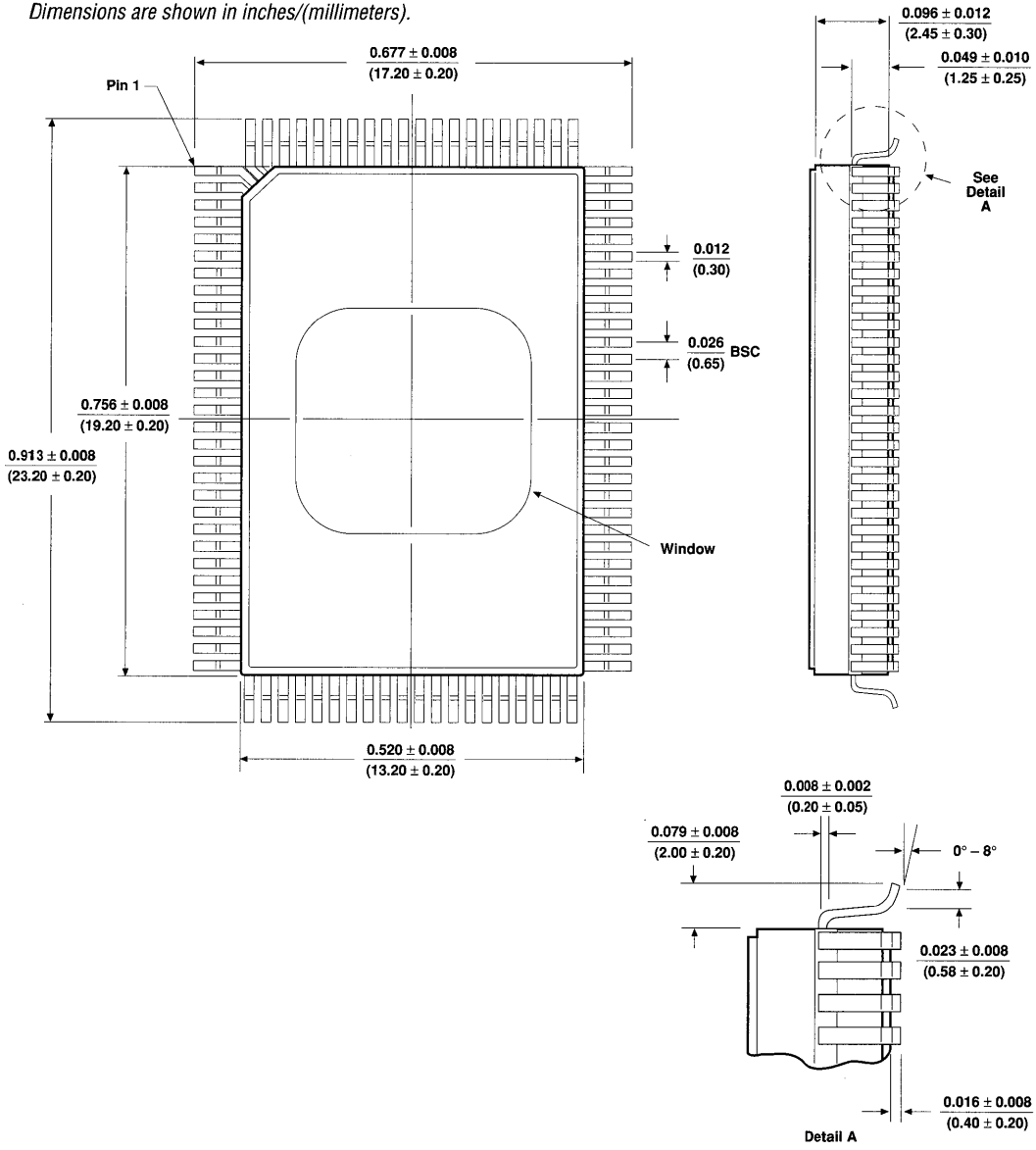
100-Pin Ceramic Pin-Grid Array (PGA)

Dimensions are shown in inches/(millimeters).



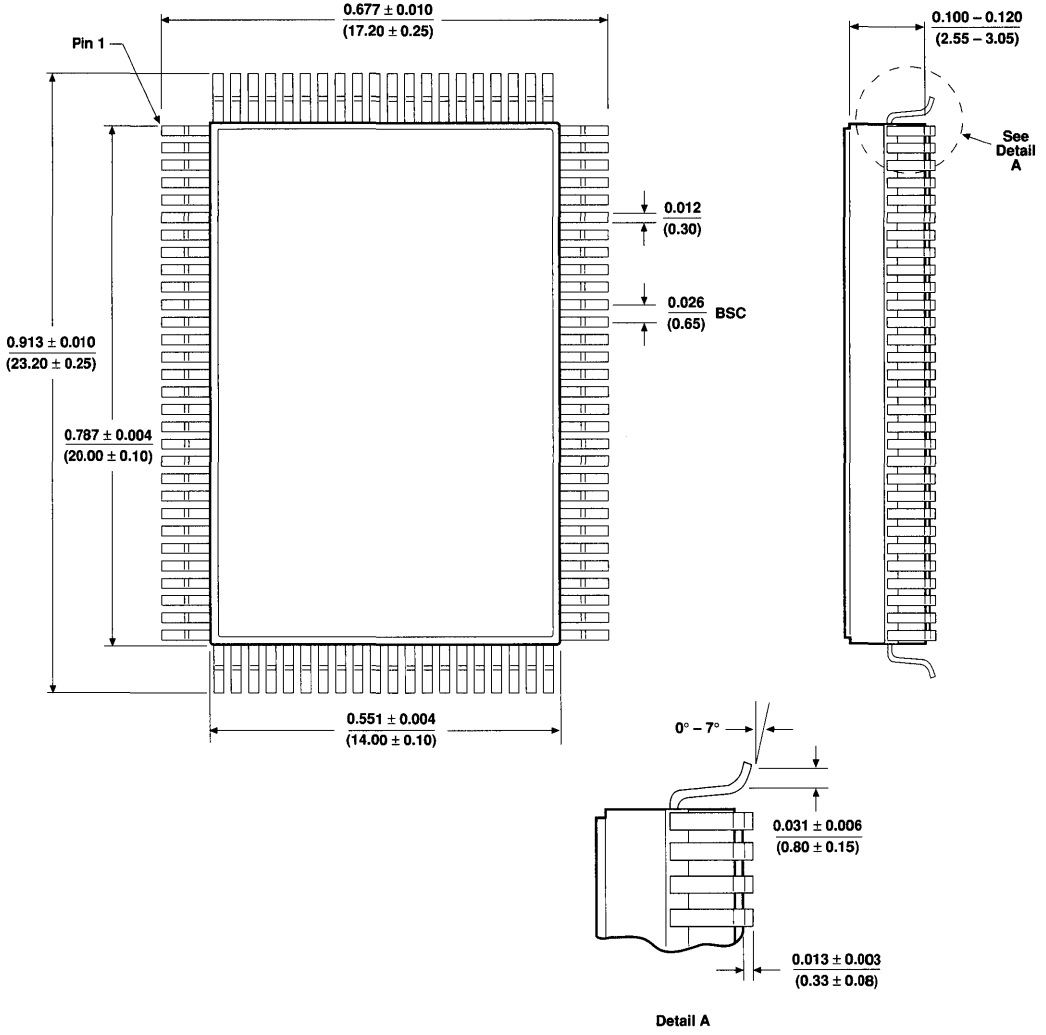
100-Pin Ceramic Quad Flat Pack (WQFP)

Dimensions are shown in inches/(millimeters).



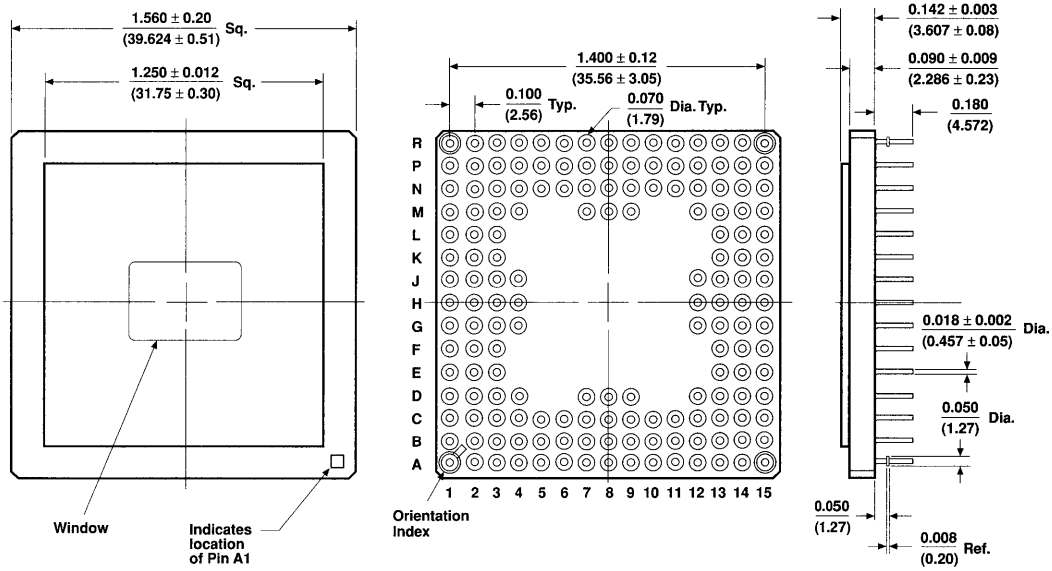
100-Pin Plastic Quad Flat Pack (PQFP)

Dimensions are shown in inches/(millimeters).



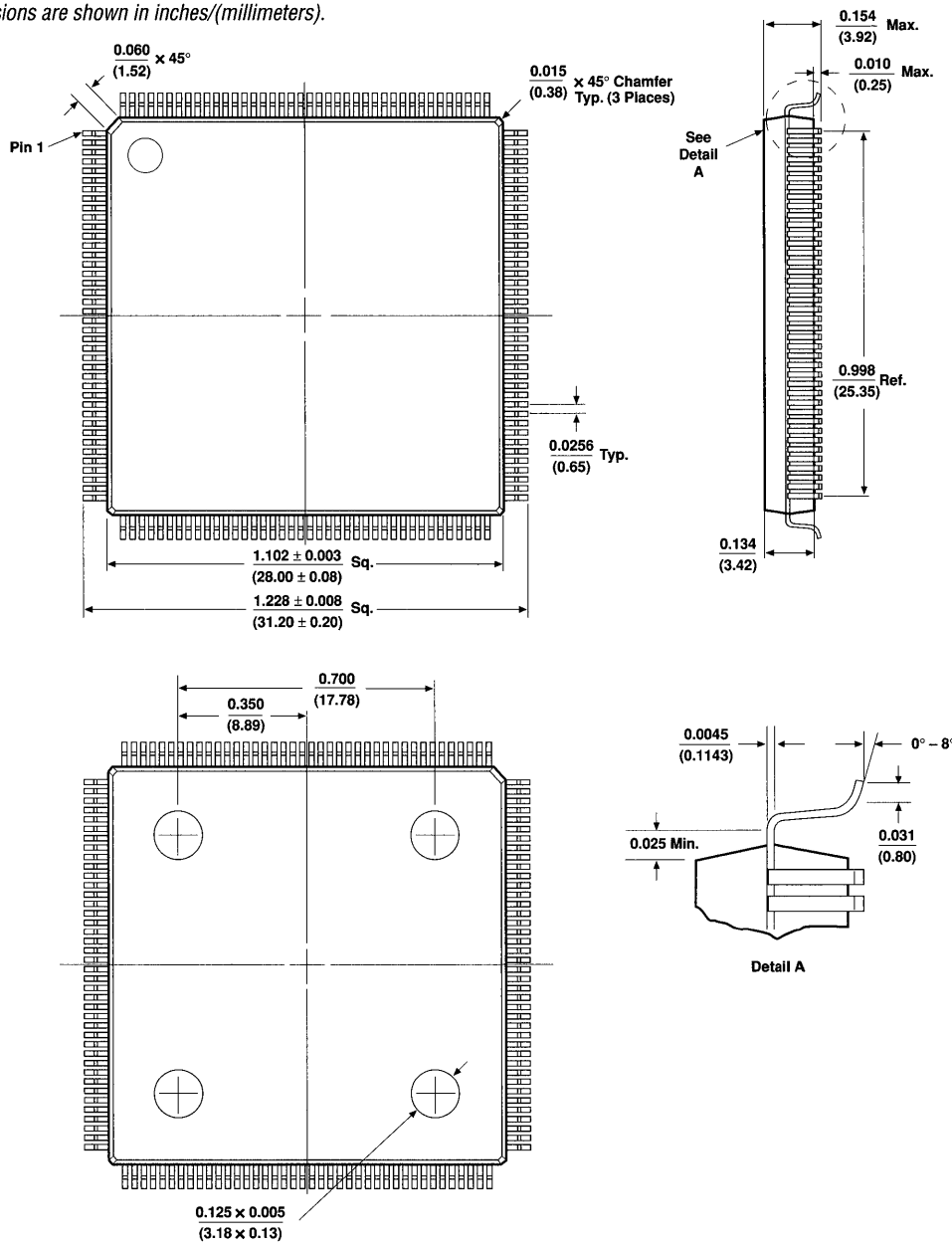
160-Pin Ceramic Pin-Grid Array (PGA)

Dimensions are shown in inches/(millimeters).



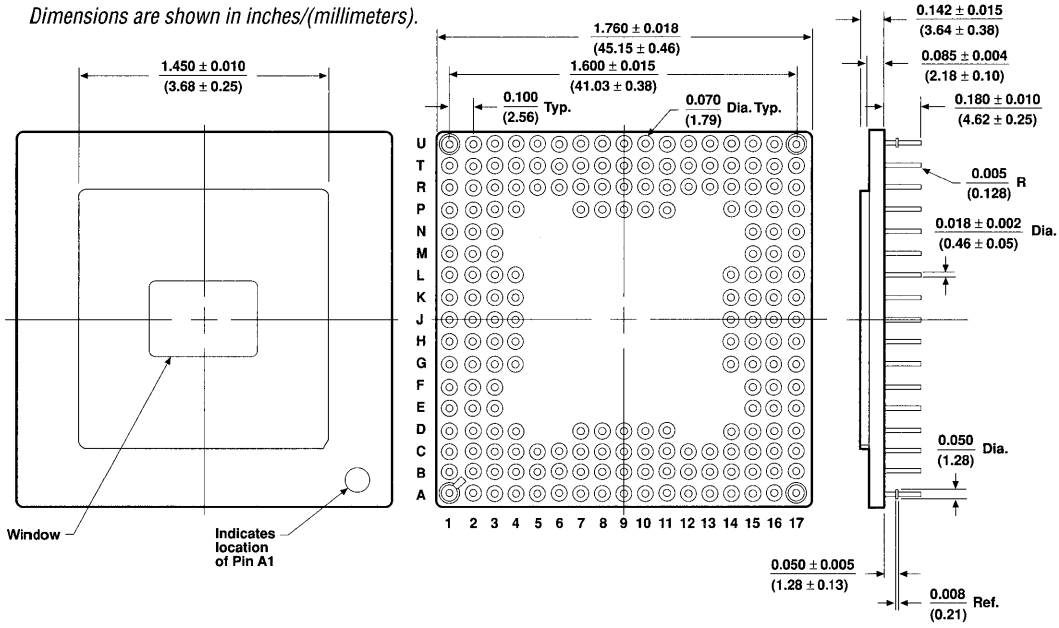
160-Pin Plastic Quad Flat Pack (PQFP)

Dimensions are shown in inches/(millimeters).



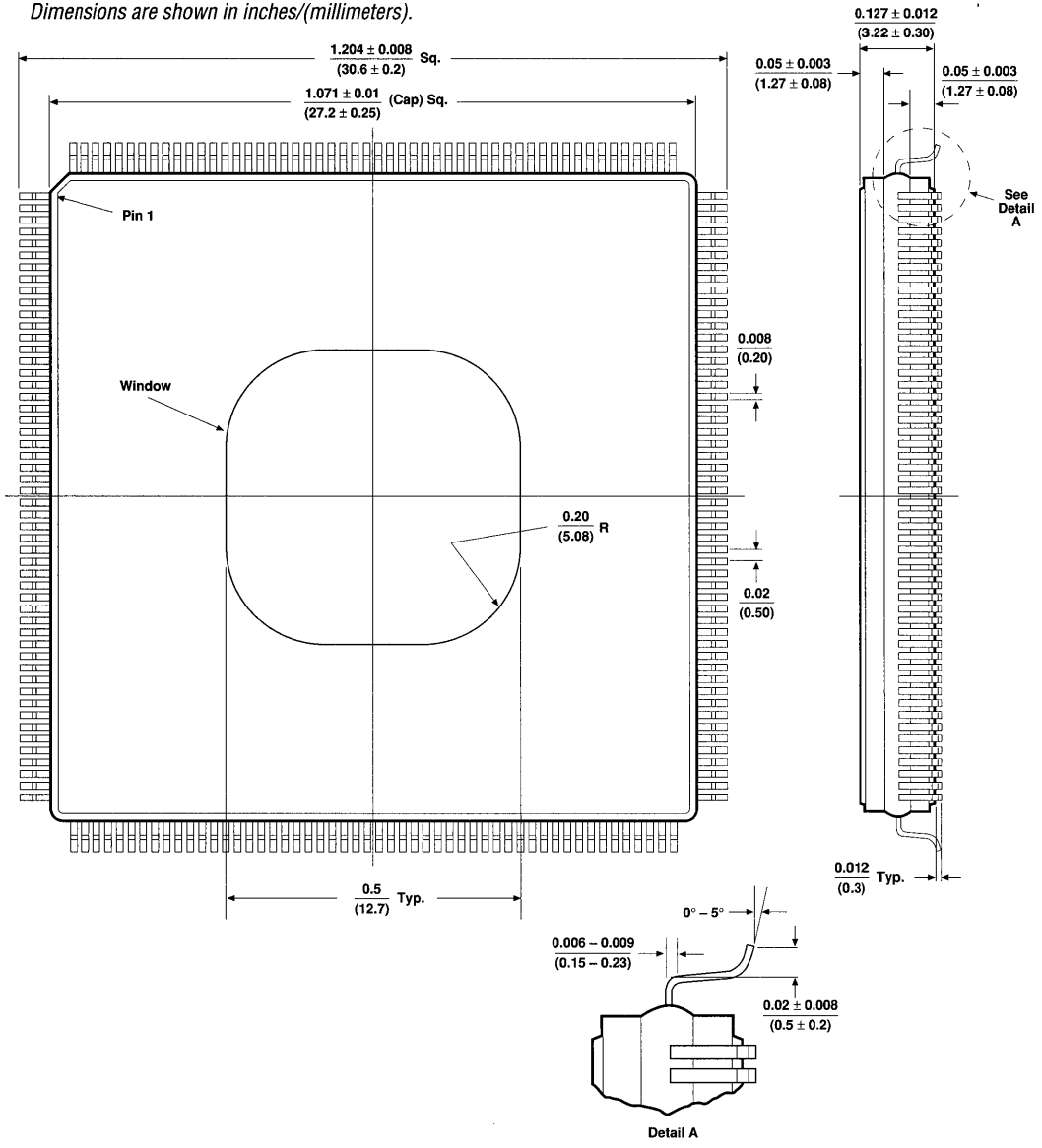
192-Pin Ceramic Pin-Grid Array (PGA)

Dimensions are shown in inches/(millimeters).



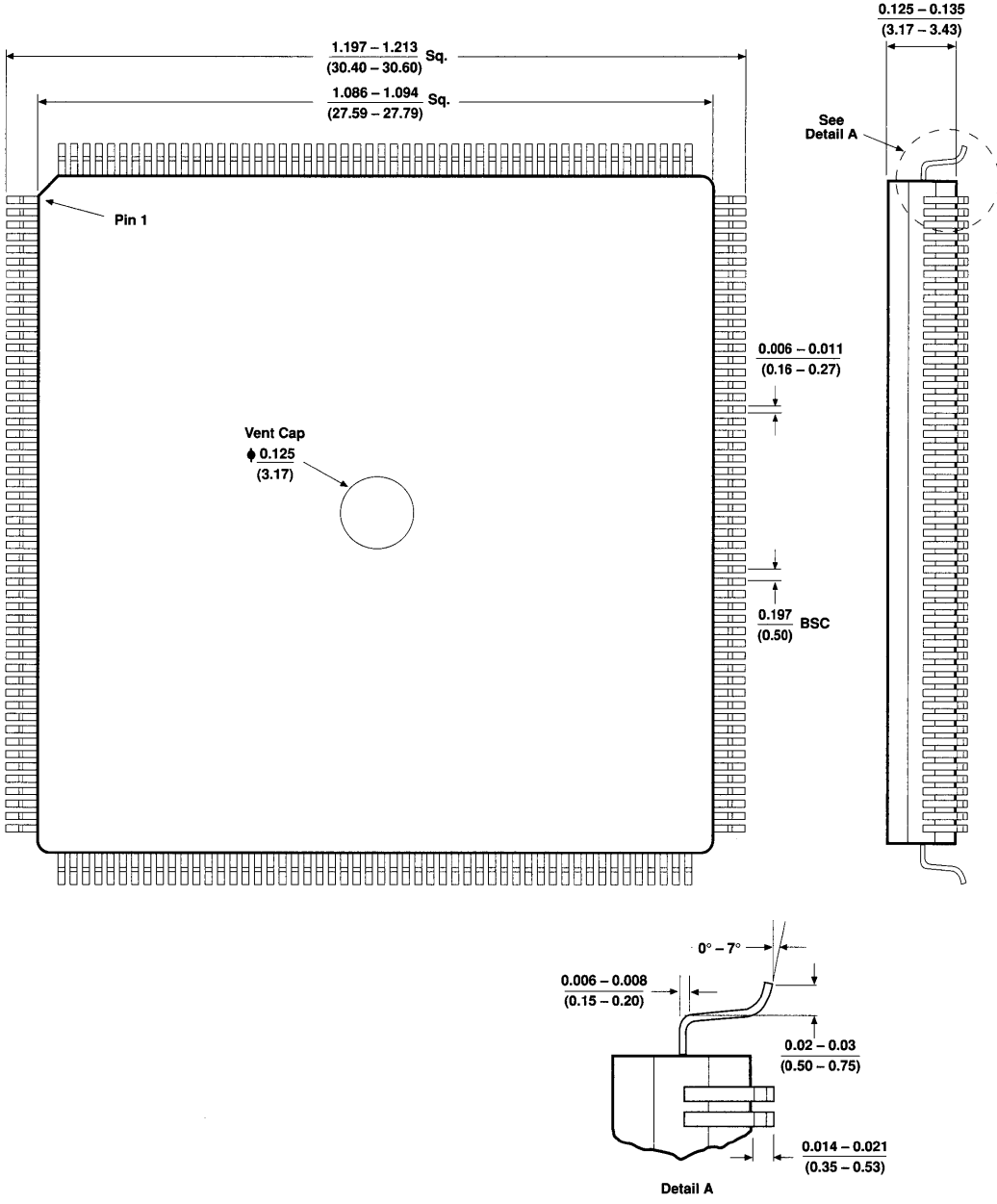
208-Pin Ceramic Quad Flat Pack (QFP)

Dimensions are shown in inches/(millimeters).



208-Pin Metal Quad Flat Pack (MQFP)

Dimensions are shown in inches/(millimeters). Where appropriate, a minimum-to-maximum range is shown.



Notes:

Electronic Bulletin Board Service

February 1993 Data Sheet

Introduction

Altera's electronic bulletin board service (BBS) provides continuous access to up-to-date device and development tool information, application notes and briefs, customer newsletters, and useful utility programs. The BBS also supports file transfers to and from the Altera Applications Engineering Department. Refer to the ***MAX+PLUS II User Guide*** (version 3.0 or higher) for detailed information on using the BBS.

Modem Number:
(408) 249-1100

The telephone number for the BBS is (408) 249-1100. To connect to the BBS via modem, the following equipment and configuration are required:

- ❑ 1200 or 2400 baud rate
- ❑ Bell Standard 212A or compatible modem
- ❑ Data format: 8 data bits, 1 stop bit, no parity

The following file transfer protocols are supported:

- ❑ ASCII (Non-Binary)
- ❑ Xmodem (Checksum)
- ❑ Xmodem-CRC (CRC)
- ❑ 1K-XModem
- ❑ Ymodem (Batch U/L and D/L)
- ❑ Zmodem (Batch U/L and D/L)
- ❑ Kermit (MS-DOS Columbia Univ.)

Logging On

After the BBS connection has been established, you can choose between graphic (for EGA or VGA displays) or non-graphic display mode. You are then prompted for your name; if you are a new user, you can also choose a password. The name and password are recorded for future log-ons.

After the Altera News and the Personal Mail screens are displayed, the Main Menu appears. From this menu, you can access all functions including on-line help for the BBS.

File Upload & Download

The File Upload service is available for uploading files that require analysis or correction by an Altera Applications Engineer. When a file is uploaded, the file description should include the name of the Altera Applications Engineer who has been asked to examine the file.

☞ All uploaded files are automatically stored in a private directory.

The BBS provides the following eight directories from which files can be downloaded:

1. *From-Altera File Directory* Used for downloading files such as customer files that have been analyzed by an Altera Applications engineer. The most recent version of programming algorithms (e.g., **mprog.exe** for MAX 5000 EPLDs and **lmap.exe** for Classic EPLDs) are also available in this directory.

2. *Engineering Application Briefs* Contains Engineering Application Briefs (EABs) and Notes (EANs) with information on using Altera devices.

3. *Engineering Application Utilities* Contains Electronic Application Utilities (EAUs) that complement Altera software and aid design. Two commonly used utilities, PLD2EQN and ABEL2MAX, are described below. All utilities are described in *Application Brief 73 (Software Utility Programs)* in the Altera 1992 ***Data Book***.

   The PLD2EQN utility converts common PAL, GAL, and PLA JEDEC Files into Altera Hardware Description Language (AHDL) Text Design Files (**.tdf**) that are compatible with the MAX+PLUS and MAX+PLUS II software. This utility can also produce an Altera Design File (**.adf**) that is compatible with A+PLUS software.

   The ABEL2MAX utility converts **.tt2** files generated by Data I/O's ABEL software (version 4.0 or higher) into AHDL TDFs that are compatible with MAX+PLUS and MAX+PLUS II software.

4. *News & Views for Altera Customers* Contains Altera newsletters that provide current news on Altera products and a "Question & Answer" section containing questions commonly asked by Altera customers.

5. *MAX+PLUS Macrofunction Exchange Library* Used for public exchange of MAX+PLUS macrofunctions. Macrofunctions in this directory can be downloaded. Macrofunctions that have been uploaded to be shared with other users are also placed here by the system operator ("Sysop").

6. *MAX+PLUS II Macrofunction Exchange Library* Used to exchange MAX+PLUS II macrofunctions in the same way as the *MAX+PLUS Macrofunction Exchange Library.*

7. *MAX+PLUS II Library Mapping Files* Used for public exchange of Library Mapping Files (**.lmf**). LMFs are used to convert EDIF netlist files generated by standard CAE development tools such as Cadence, Mentor Graphics, Minc, OrCAD, Synopsys, and Viewlogic into a MAX+PLUS II-compatible format.

8. *Data I/O Support for Altera Devices* Lists the Data I/O software and hardware that can be used to program Altera devices.

Ordering Information

February 1993

Ordering Altera Devices

Figure 1 explains the device ordering code for Altera devices. Since many devices are available with different pin counts for the same package type, the ordering code includes pin count. Most devices use relative numbers (e.g., -1, -2) to designate speed grades, while others use actual propagation delay times (e.g., -15, -20). For information on specific package, speed grade, and operating temperature combinations, refer to individual device data sheets in this data book, or contact Altera Marketing at (408) 894-7000.

Figure 1. Device Package Ordering Codes

EPM 7032 L C 44 -3 T

Family Signature:
- EP: Classic device
- EPM: MAX 5000 or MAX 7000 device
- EPF: FLEX 8000 device
- EPC: Configuration EPROM device
- EPS: EPS464 or SAM device
- EPB: Micro Channel device

Device Type:
- EP: 320, 330, 610, 610A, 610T, 630, 910, 910A, 910T, 1810, 1810T, 1830
- EPM: 5016, 5032, 5064, 5128, 5130, 5192, 7032, 7032V, 7064, 7096, 7128, 7160, 7192, 7256
- EPF: 8452, 8820, 81188
- EPC: 1064, 1213
- EPS: 448, 464
- EPB: 2001, 2002A

Package Type:
- D: Ceramic dual in-line package (CerDIP)
- P: Plastic dual in-line package (PDIP)
- J: Ceramic J-lead chip carrier (JLCC)
- L: Plastic J-lead chip carrier (PLCC)
- G: Ceramic pin-grid array (PGA)
- S: Plastic small-outline integrated circuit (SOIC)
- W: Ceramic quad flat pack (WQFP), *Note (1)*
- M: Metal quad flat pack (MQFP), *Note (1)*
- Q: Plastic quad flat pack (PQFP), *Note (1)*
- T: Thin quad flat pack (TQFP), *Note (1)*

Pin Count:
Number of pins for devices with different pin-count options (MAX 7000, FLEX 8000, and Configuration EPROM devices only)

Operating Temperature/Military Processing:
- C: Commercial temperature (0° C to 70° C)
- I: Industrial temperature (–40° C to 85° C)
- M: Military temperature (–55° C to 125° C)
- M883B: Processed to MIL-STD-883, current revision
- M883BX: Processed to MIL-STD-883, current revision with modified J-lead package dimension
- MB: Fully compliant with deviation to MIL-STD-883, current revision (consult Altera for specific deviations)
- 5962: DESC Standard Military Drawing (SMD)

Speed Grade:
See individual data sheets in this data book for speed/product relationships (e.g., -15, -20, or blank).

Turbo Bit Option:
Indicates Turbo Bit option preset at the factory

Examples:

EPF81188GC232-3 EPF81188 in a ceramic 232-pin PGA package, commercial temperature range, -3 speed grade

EPM5130GM883B EPM5130 in a ceramic 84-pin pin-grid array package, MIL-STD-883B-qualified

Note:

(1) MAX 5000 and MAX 7000 devices in QFP packages with 100 or more pins are shipped in QFP carriers. For more information on QFP carriers, see the *QFP Carrier & Development Socket Data Sheet* in this data book.

MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs) available from Altera Marketing. These MPDs should be used to prepare Source Control Drawings (SCDs).

Ordering Development Tools

Table 1 provides ordering codes for Altera's MAX+PLUS II development systems and software and lists the Altera devices supported by each configuration. To order a development system with PS/2-compatible hardware, append "/PS" to the ordering code (e.g., PLDS-HPS/PS).

Table 1. Altera Development Systems, Software & Device Support

Ordering Codes	Design Entry				Compilation & Verification								Device Support		
	Schematic Capture	Waveform Design Entry	Text Design Entry	EDIF Interface	Design-Rule Checking	Functional Simulation	Timing Simulation	Multi-Device Simulation	Multi-Device Partitioning	Timing Analysis	Waveform Editing	Programming Hardware	FLEX 8000	MAX 7000	MAX 5000/EPS464	Classic Note (1)
Base Systems (PC Platform)																
PL-ASAP2												✓	✓	✓	✓	✓
PLS-ADV	✓	✓		✓						✓				✓	✓	✓
PLS-ES	✓	✓		✓						✓						✓
PLS-FLEX8	✓	✓		✓						✓			✓		✓	✓
PLS-HPS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓
PLS-STD	✓	✓		✓						✓					✓	✓
PLDS-HPS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓
Add-On Products (PC Platform)																
PLSM-5K														✓	✓	
PLSM-7K													✓			
PLSM-8K												✓				
PLSM-ADE			✓		✓	✓	✓	✓	✓		✓					
Base Systems (Workstation Platform)																
PLS-FLEX8/HP		✓		✓		✓						✓		✓	✓	
PLS-FLEX8/SN		✓		✓		✓						✓		✓	✓	
PLS-WS/HP		✓		✓		✓						✓	✓	✓	✓	
PLS-WS/SN		✓		✓		✓						✓	✓	✓	✓	
Add-On Products (Workstation Platform)																
PLSM-7K/WS														✓		

Note:
(1) EPM5016, EPM5032, and EPM7032 devices are also supported with Classic devices.

Ordering a Software Maintenance Agreement

Renewable, one-year software maintenance agreements for development products provide software and documentation updates for all registered owners of Altera development systems. Table 2 shows the codes for ordering software maintenance agreements.

Table 2. Software Maintenance Agreement

Product	Ordering Code
PLS-ES	PLAESW-ES
PLS-STD	PLAESW-STD
PLS-ADV	PLAESW-ADV
PLS-FLEX8	PLAESW-FLEX8
PLS-HPS, PLDS-HPS	PLAESW-HPS
PLSM-5K	PLAESW-5K
PLSM-7K	PLAESW-7K
PLSM-8K	PLAESW-8K
PLSM-ADE	PLAESW-ADE
PLS-FLEX8/SN, PLS-FLEX8/HP	PLAESW-FLEX8/WS
PLS-WS/SN, PLS-WS/HP	PLAESW-WS
PLSM-7K/WS	PLAESW-7K/WS

Ordering Programming Hardware & Adapters

This section provides the ordering codes for Altera programming hardware. Table 3 lists the ordering codes for the programming card and units.

Table 3. Programming Hardware

Product	Ordering Code	Description
LP6 Logic Programmer Card	PLP6	Interfaces with IBM PC-AT or compatible computer.
Master Programming Unit (MPU)	PL-MPU	Directly programs EP320 and EP330 DIP devices; adapters are required to program all other devices.
Altera Stand-Alone Programmer	PL-ASAP2	Includes programming software, a Logic Programmer card, and the MPU. To order a package with programming hardware that supports IBM PS/2 and compatible computers, append "/PS" to the end of the ordering code.

Table 4 lists the ordering codes for programming adapters. The Master Programming Unit (MPU) supports both PLE- and PLM-type programming adapters. PLE-type adapters provide programming support; PLM-type adapters provide programming support, device-to-socket continuity testing, and device functional testing.

Table 4. Device Adapter Support (Part 1 of 2)

Device *Notes (1), (2)*	**Package**	**Adapter** *Note (3)*
EP310, EP320	DIP	None required
EP330	DIP J-Lead SOIC	None required PLEJ330 PLES330
EP600/610/610T/630	DIP J-lead SOIC	PLED610 PLEJ610 PLES610
EP900/910/910A/910T	DIP J-lead	PLED910 PLEJ910
EP1800/1810/1810T/1830	J-lead PGA	PLEJ1810, PLMJ1810 *(4)* PLEG1810
EPB2001	J-lead	PLEJ2001
EPM5016	DIP J-lead SOIC	PLED5016 *(5)* PLEJ5016 *(5)* PLES5016 *(5)*
EPM5032	DIP J-lead SOIC	PLED5032 *(5)*, PLMD5032 *(4)* PLEJ5032 *(5)*, PLMJ5032 *(4)* PLES5032 *(5)*
EPM5064	J-lead	PLEJ5064 *(5)*, PLMJ5064 *(4)*
EPM5128	J-lead PGA	PLEJ5128 *(5)*, PLMJ5128 *(4)* PLEG5128 *(5)*
EPM5130	J-lead PGA QFP	PLEJ5130 *(5)*, PLMJ5130 *(4)* PLEG5130 *(5)* PLMQ5130 *(4)*
EPM5192	J-lead PGA	PLMJ5192 *(4)* PLMG5192 *(4)*
EPM7032, EPM7032V	J-lead QFP TQFP	PLMJ7032-44 *(4)* PLMQ7032-44 *(4)* PLMT7032-100 *(4)*
EPM7064	J-lead PQFP	PLMJ7064-68 *(4)* PLMQ7064-100 *(4)*
EPM7096	J-lead (68-pin) J-lead (84-pin) QFP	PLMJ7096-68 *(4)* PLMJ7096-84 *(4)* PLMQ7096-100 *(4)*

Table 4. Device Adapter Support (Part 2 of 2)

Device *Notes (1), (2)*	Package	Adapter *Note (3)*
EPM7128	J-lead QFP (100-pin) QFP (160-pin)	PLMJ7128-84 *(4)* PLMQ7128-100 *(4)* PLMQ7128-160 *(4)*
EPM7160	J-lead QFP	PLMJ7160-84 *(4)* PLMQ7160-160 *(4)*
EPM7192	PGA QFP	PLMG7192-160 *(4)* PLMQ7192-160 *(4)*
EPM7256	PGA QFP	PLMG7256-192 *(4)* PLMQ7256-208 *(4)*
EPF8452	PGA	PLMG8452-160 *(4)*
EPF8820	PGA	PLMG8820-192 *(4)*
EPF81188	PGA	PLMG81188-232 *(4)*
EPC1064	DIP J-lead	Any FLEX 8000 adapter Any FLEX 8000 adapter
EPC1213	DIP J-lead	Any FLEX 8000 adapter Any FLEX 8000 adapter
EPS448	DIP J-lead	PLED448 PLEJ448
EPS464	J-lead QFP	PLEJ464, PLMJ464 *(4)* PLEQ464, PLMQ464 *(4)*

Notes:

(1) All devices except MAX 7000 and FLEX 8000 devices can be programmed with the PL-MPU or PLE3-12A programming unit. MAX 7000 and FLEX 8000 devices can be programmed only with the PL-MPU unit.
(2) The LP4, LP5, or LP6 programming card can be used with all devices.
(3) Refer to the *PLED/J/G/S/Q & PLMD/J/G/S/Q Data Sheet* in the Altera 1992 ***Data Book*** for more information.
(4) This adapter supports functional testing and continuity checking and can be used only with the PL-MPU programming unit.
(5) These adapters are labeled with an "A" suffix (e.g., PLED5032A).

Ordering QFP Carriers & Sockets

Table 5 shows the ordering codes for QFP device development sockets. All MAX 5000/EPS464 and MAX 7000 QFP devices with 100 or more pins are shipped in carriers.

Table 5. QFP Device Sockets

Product	Ordering Code
100-pin development socket	PL-SKT/Q100
160-pin development socket	PL-SKT/Q160
208-pin development socket	PL-SKT/Q208

Notes:

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February 1993

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Robert Electronic Sales
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FAX: (301) 964-3364

FLORIDA
EIR, Inc.
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Maitland, FL 32751
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FAX: (407) 660-9091

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WLA & Associates
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Lawrenceville, GA 30243
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AEM, Inc.
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Oasis Sales Corporation
1101 Tonne Road
Elk Grove Village, IL 60007
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INDIANA
Electro Reps, Inc.
7240 Shadeland Station, Suite 275
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FAX: (317) 841-0230

IOWA
AEM, Inc.
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Rathsburg Associates, Inc.
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Cahill, Schmitz & Cahill, Inc.
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Premier Technical Sales
23566 Woodhaven Place
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TEL: (916) 268-3357
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OASIS
301 E. Bethany Home Road #A135
Phoenix, AZ 85012
TEL: (602) 277-2714
FAX: (602) 268-9352

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ERA, Inc.
354 Veterans Memorial Highway
Commack, NY 11725
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FAX: (516) 543-0758

NEW MEXICO
Nelco Electronix
3240 C Juan Tabo Blvd. NE
Albuquerque, NM 87111
TEL: (505) 293-1399
FAX: (505) 293-1011

NEW YORK
ERA, Inc. (New York Metro)
354 Veterans Memorial Highway
Commack, NY 11725
TEL: (516) 543-0510
FAX: (516) 543-0758

Technology Sales, Inc.
920 Perinton Hills Office Park
Fairport, NY 14450
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FAX: (716) 223-5526

NORTH CAROLINA
WLA & Associates
5337 Trestlewood Lane
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The Lyons Corporation
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FAX: (206) 453-8758

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FAX: (612) 646-4484

Oasis Sales Corporation
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FAX: (414) 782-7921

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Compass Marketing
5600 S. Quebec Street, Suite 3500
Englewood, CO 80111
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FAX: (303) 721-0195

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Kaytronics
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Calgary, Alberta T2E 7H7
Canada
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BRITISH COLUMBIA
Kaytronics
#102-4585 Canada Way
Burnaby, BC V5G 4L6
Canada
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ONTARIO
Kaytronics
331 Bowes Road, Unit 1
Concord, Ontario L4K 1J2
Canada
TEL: (416) 669-2262

Kaytronics
300 March Road, Suite 603
Kanata, Ontario K2K 2E2
Canada
TEL: (613) 564-0087

QUEBEC
Kaytronics
5800 Thimens Boulevard
Ville St. Laurent, Quebec H4S 1S5
Canada
TEL: (514) 745-5800

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ARGENTINA
YEL S.R.L.
Virrey Cevallos 143
1077 Buenos Aires
Argentina
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TLX: (390) 18605 (YEL AR)
FAX: (54) 1-476-2551

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Veltek Pty. Ltd.
18 Harker St.
Burwood, Victoria 3125
Australia
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FAX: (61) 3-808-5473

AUSTRIA
Hitronik
St.-Veit-Gasse 51
1130 Wien
Austria
TEL: (43) 222-824-199
TLX: (847) 134404 (HIT)
FAX: (43) 222-828-557-2

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D&D Electronics
VIIe Olympiadelaan 93
2020 Antwerpen
Belgium
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TLX: (846) 73121 (DDELEC BU)
FAX: (32) 3-828-7254

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Uniao Digital Ltda.
Rua Georgia 69
04559-010
São Paulo - SP
Brazil
TEL: (55) 11 533-0966
FAX: (55) 11 533-6780

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CIDC
P.O. Box 729
Xia Guang Li No. 9
Sanyuanqiao, Dongzhimenwai
Beijing 100016
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E.V. Johanssen Elektronik A/S
Titangade 15
2200 Koebenhavn N
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TLX: (855) 16522 (EVICAS DK)
FAX: (45) 31 83 92 22

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SF-02201 Espoo
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FAX: (358) 0-452-3337

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FAX: (33) 1 45 07 21 91

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Vertriebs-AG
Stahlgruberring 12
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TLX: (841) 522561 (ELEC D)
FAX: (49) 89/45110-129

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A16, 6/F Proficient Industrial Center
6 Wang Kwun Road
Kowloon
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FAX: (852) 305-0640

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Sritech Information Technology Ltd.
744/51, 2nd Floor, Chintal Plaza
33rd Cross, 10th Main
4th Block, Jayanagar
Bangalore 560 011
India
TEL: (91) 812-640-661
TLX: (953) 08458162 (SRIS IN)
FAX: (91) 812-633-508

Capricorn Systems International
1340 Tully Road
San Jose, CA 95122
TEL: (408) 294-2833
FAX: (408) 294-0355

IRAN
BBS Electronics Pte. Ltd.
1 Genting Link
Perfect Industrial Building #05-03
Singapore 1334
TEL: 65-748-8400
FAX: 65-748-8466

ISRAEL
Active Technologies
2200 Marcus Avenue
New Hyde Park, NY 11402
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TEL: (516) 488-1226
FAX: (516) 488-1245

Vectronics Ltd.
60 Medinat Hayehudim Street
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Herzlia B 46120
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TLX: (922) 342579 (VECO IL)
FAX: (972) 52-556-508

ITALY
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Viale Fulvio Testi, 208
29126 Milano
Italy
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FAX: (39) 2 661 01385

JAPAN
Altima Corporation
Hakusan High-Tech Park
1-22-2 Hakusan, Midori-Ku
Yokohama City 226
Japan
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FAX: (81) 45-939-6114

Paltek Corporation
5-2-12 Kamiyoga
Setagaya-Ku
Tokyo 158
Japan
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TLX: (781) 02425205 (PALTEK J)
FAX: (81) 33-707-5338

KOREA
MJL Korea, Ltd.
Bookook Security Building
34-2 Youido Dong
Yeungdeungpo Ku
Seoul, 150-010
Korea
TEL: (82) 2-784-8000
TLX: 843457 (MJL MORV)
FAX: (82) 2-784-4644

Rosedale Business Group
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Princeton, NJ 08540
USA
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FAX: (609) 683-7447

MEXICO
Intectra
Avenida 1, #100
Col. San Pedro de los Pinos
Mexico 03800, D.F.
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FAX: 52 2 516 2468

NETHERLANDS
Koning en Hartman
1 Energieweg
2627 AP Delft
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TLX: 38250 (KOHA NL)
FAX: (31) 15 619194

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Eltron A/S
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0753 Oslo 7
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FAX: (65) 286-1812

SPAIN
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Paseo de la Habana, 190
28036 Madrid
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FAX: (46) 8 83 69 18

SWITZERLAND
Eljapex AG
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5430 Wettingen
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FAX: (41) 56 26 14 86

TAIWAN
Galaxy Far East Corp.
8F-6, 390 Sec. 1
Fu Hsing South Road
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Taiwan R.O.C.
TEL: (886) 2-705-7266
TLX: (785) 26110 (GALAXYER)
FAX: (886) 2-708-7901

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Thame, Oxon 0X9 3UQ
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